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On the Cover....
Two of 6 wires (A and C) in the microcircuit were found to be broken at the heels of die bonds after relatively mild screening. Fracture surfaces indicated they were very brittle breaks. The other bonds in this part and all bonds in two from the same lot were normal. The peening seen in the closeup of wire A indicates that the cause was extensive cyclic stress at a relatively low level consistent with ultrasonic energy. One theory is that the wire bonding tool was not shut off immediately after the bonds were made. Another is that the parts were ultrasonically cleaned, which is not a recommended process for electronic parts.
(Picture and description courtesy of Tom Brennan of the GSFC Parts Analysis Laboratory)

WWW URL Address:

http://arioch.gsfc.nasa.gov/eee_links/eeeintro.html

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LETTER FROM THE EDITOR

by Melanie Ott
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In keeping with the trend of growth and change, I too will be moving on to new opportunities and want to say "farewell" to the *EEE Links* readers. It has been a pleasure serving you and I want to thank you very much for your support.

In the October issue of *EEE Links* you will receive information concerning the new editorial/publishing staff. If you would like to contact me in the future please use the email address: melanie.n.ott.1@gsfc.nasa.gov and you will always be able to reach me on center. For all mailing list information please contact Sid Brashears at 301-731-8917 or sidney.s.brashears.1@gsfc.nasa.gov. You can access *EEE Links* on the World Wide Web at: http://arioch.gsfc.nasa.gov/eee_links/eeeintro.html

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QUALITATIVE REAL-TIME ESTIMATION OF PARTICULATE FALLOUT CONTAMINATION IN CLEANROOMS

by Paul Mogen,
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Measurement of contamination deposition levels on surfaces such as payload optics is critical to assuring that the payload's functionality is not impaired. Currently at NASA, Kennedy Space Center, these measurements were performed by placing a 37 millimeter diameter gridded filter near a payload for two weeks and then manually counting and sizing the contamination using an optical microscope in a laboratory. This method is manpower intensive and subject to human errors.

A real-time particle fallout monitor was developed in the NASA Contamination Monitoring Laboratory for use in operational clean work areas at Kennedy Space Center. This device is a qualitative measure of the total amount of contamination by monitoring the amount of light scattered by particles which deposit on a mirror surface in the instrument.

This device has been field tested in the Operations & Checkout building at KSC. It was found to correlate well with scheduled activities in the test area. It will be turned over to Payload operations personnel for evaluation and subsequently to Shuttle operations.

Work has also been done on this project in order to produce a quantitative device which will count and size fallout contamination. This device was developed during fiscal year 1996 and is currently being field tested.

This device also has applicability to the microelectronics industry for monitoring micro-environments for cleanliness and indications of contamination in process equipment.

Additional information can be found at:
http://www-de.ksc.nasa.gov/de/dl/dl-icd/cml_lab/QUALOFM.html

ALLEN-BRADLEY TO PHASE OUT CARBON COMPOSITION FIXED RESISTOR BUSINESS

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On May 17, 1996 Rockwell Automation, parent company of Allen-Bradley, announced that it will phase out its carbon composition fixed resistor business, located in El Paso, TX. This decision was made based upon a steady decline in worldwide demand for this resistor type. Carbon composition resistor technology is more than 30 years old and is rapidly being replaced by smaller, less expensive devices like metal film resistors.

Allen Bradley is currently the only military qualified source of the commonly used RC and RCR style resistors made to MIL-R-11 and MIL-R-39008 respectively. Customers will be able to place orders through August 15 with delivery of the product expected to continue into early 1997.

The Passive parts Supplier Assessment Program (PSAP) at Goddard Space Flight Center is preparing a formal NASA Parts Advisory on this issue to alert NASA programs of the impending loss of the only supplier of QPL carbon composition resistors. The Advisory will provide recommendations for potential alternate part types to meet form, fit, function and reliability requirements.

THERMO-MECHANICAL STRESS ANALYSIS OF AN MCM-D INTERCONNECT

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Abstract
Temperature cycling stresses within the interconnect structure of a multichip module substrate were examined using a two-dimensional, plane-strain finite element model. An intermetallic via within the substrate was analytically exercised through a series of temperature excursions, and the resulting cyclic strain range was determined. This strain range was then used to predict cyclic fatigue life for the hybrid device, using the Coffin-Manson fatigue relation. The life prediction was ultimately compared with results of thermal cycle testing conducted at the Naval Surface Warfare Center, Crane Division (NSWC Crane), under the auspices of the Reliability Technology to Achieve Insertion of Advanced Packaging (RELTECH) program.
Keywords: hybrid, via fatigue, finite element analysis

TOTAL-DOSE RADIATION PERFORMANCE OF INTERPOINT DC-TO-DC CONVERTERS

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A Parts Technology Report number 54678 was published by GSFC in August, 1995, reporting the results of four different types of Interpoint DC-to-DC converters as follows: MFL2805S, MFL2815S, MFL2812S and MFL2815D. The Lot Date Codes for these parts were 9442 and 9443. Recently, two Interpoint DC-to-DC converters, namely MHF2812D and MHF2805S, procured for the CASSINI Project with a LDC of 9603 were total-dose radiation tested at a low dose rate of 100 rads(Si)/hour up to 50 krads(Si). The MHF2812D parts passed all electrical tests throughout the radiation testing to 50 krads(Si), however the MHF2805S parts showed significant degradation in Vout Full Load at 20, 30 and 50 krads(Si). However, under limited testing and half-load conditions, the parts passed most of the tests up to 30 krads(Si).

A copy of the Parts Technology Report (# 54678), as well as radiation report # PPM-96-004, which provides the details of the radiation testing, can be obtained by contacting the NASA/Goddard Space Flight Center Office of Flight Assurance (OFA) Information Center, (301) 286-7240.

THE RADIATION EFFECTS AND ANALYSIS HOME PAGE

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The Radiation Effects and Analysis Group at NASA-GSFC is now on-line! Our World Wide Web page spans as diverse a range of subjects as the group itself does: Single Event Effects (SEE), Total Ionizing Dose(TID), the space radiation environment and the Radiation Physics Office (RPO), radiation-related flight projects and flight data analysis, and other radiation-related groups and conferences.

The page was designed to be useful for designers, parts engineers, project managers, other radiation groups, and anyone else with an interest. Tutorial-style descriptions, relevant papers and documents, and useful links are available on all subjects. In addition, we've moved our SEE test database on-line; information currently available includes a list of devices we've tested with the results and recommendations, test reports, and upcoming testing planned.

Come visit our site at:
http://flick.gsfc.nasa.gov/radhome.htm

REDUCTION OF CALCOFLUOR IN SOLITHANE CONFORMAL COATINGS

by Michael K. Miller Lt. USAF (724.4)
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Abstract
An investigation on the outgassing of a pigment employed as a fluorescent medium in conformal coatings has been performed. The conformal coatings in question are used to protect printed wiring boards from environmental hazards such as dust and moisture. The pigment is included in the coating at low concentration to allow visual inspection of the conformal coating for flaw detection. Calcofluor, the fluorescent pigment has been found to be a significant outgasser under vacuum conditions and a potential source of contamination to flight hardware. A minimum acceptable concentration of Calcofluor for flaw detection is desirable. Tests were carried out using a series of Solithane™ conformal coating samples, with progressively

lower Calcofluor concentrations, to determine the minimum required concentration of Calcofluor. It was found that the concentration of Calcofluor could be reduced from 0.115% to 0.0135% without significant loss in the ability to detect flaws, while at the same time significant reductions in Calcofluor outgassing and possible contamination of systems could be realized. For further information please contact John Scialdone at GSFC Code 313, 301-286-6731, or at John.J.Scialdone@gsfc.nasa.gov.

COMPOSITE MATERIAL BEHAVIOR UNDER APPLIED ELECTRIC FIELD

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ABSTRACT

Current-voltage characteristics of the electrically conductive silver-filled epoxy Ablefilm ECF-563 preform switches to a high-resistive state under low bias voltage. The observed phenomena is argued to be an intrinsic property of electrically conducting composite materials caused by strong localized centers that introduce space charge.

INTRODUCTION

Electrically conductive silver-filled epoxy preform, ECF-563 Ablefilm [1], is used in an Ultra High Frequency (UHF) power amplifier circuitry as shorting pads for very small (0.055 in. diameter) cross-sectional circuit elements. The circuit functions under a pulse condition in which multiple pin diodes switch to on/off positions. The UHF power amplifier developed some intermittent behavior which was traced to switching in the epoxies under the pin diodes. This paper describes a set of tests which were performed on ECF-563 preform samples for the purpose of understanding the switching phenomena and to propose a relevant transport model. We observed intermittent switching to a high-resistive state in silver-filled epoxy preform Ablefilm ECF-563 under an applied voltage. For a 0.003-in. thick sample of ECF-563 sandwiched between two gold contacts, a threshold voltage of 0.4-1.9 V exists for switching to a high-resistive state. This observation raises a concern regarding the use of ECF-563 in hybrid microelectronics.

Additional switching to a high-current-carrying state was also observed in the same material under higher applied voltage. These phenomena appear not to involve damage to the material (although they can be accompanied by some incidental damage). Understanding of the switching mechanisms will enable reliability enhancement of hybrid circuits and application of these materials to control detrimental effects of ESD and electrical surges.

We have searched the literature on switching instability and intermittent behavior of materials to identify the contributing transport mechanism. The models and their features are briefly introduced.

A thin layer of an insulator sandwiched between metal electrodes frequently possesses special electrical switching properties that at first can be dismissed as dielectric breakdown. The phenomena of "forming" (a reproducible change in electrical conductivity induced by a high electric field) is different from arcing or destructive dielectric breakdown phenomena.

There are numerous articles in the literature on the phenomena of switching in metal-insulator-metal (MIM) junctions (with thin insulators). This subject was considered mostly during the 60s and 70s and is covered in review articles [2,3]. "Forming" governs the behavior of as-manufactured MIM junctions exhibiting switching, which do not require electrical pretreatment ("electroforming"). The current-voltage characteristics of these MIM junctions exhibit S-type or N-type nonlinearity with negative differential resistance (NDR) behavior. The most popular theory, explaining the above mentioned phenomena, is carbonaceous filamentation and its rupture indicative of S-type instability. There is no simplified theory that can describe N-type instability. Although some physical evidence for the filament formation has been reported in the literature, e.g., via chemical vapor decoration [9], a comprehensive microscopic theory governing both S-type and N-type phenomena in MIM junctions is desired. Both instabilities have been observed in a variety of MIM junctions and composites of metal particles in an insulator background; metals vary over a wide range (Ag, Al, Au, Pt, Si, Nb, Be, Mg, Cu, Zn, Ti, Cr, Mn, Fe, Co, Ni, In, Zr, Sn, Pb, Bi, W) and insulators vary from polymers (styrene, acetylene, analine) to oxides (SiOx, AlOx, NbOx, TiOx, CrOx, VOx, TaOx, CuOx, MgO) and others (AlNx,..). Common among all these systems is metal entities separated by a thin dielectric film. The insulator film is undoubtedly far from an ideal pure dielectric. One can easily envision the presence of defects, traps, and localized centers in the dielectric. Polymers contain dangling bonds, broken chains, free radicals, spin and charge defects, dopants, etc. Oxides fabricated via fast and cheap industrial processes possess a well-exhibited space charge [10] and are far from single crystalline oxides used in some of the MIM junction studies mentioned previously. In a typical system, electrons can transfer from one metal entity to another through a variety of mechanisms. These mechanisms involve inelastic interaction of electrons with the defects present in the dielectric material and, therefore, lead to excess heating, runaway phenomena, and dielectric breakdown.

A microscopic picture of the conduction mechanism in thin disordered materials is developed in [11]. The authors emphasize the role played by deep localized trap centers in capturing transit-free carriers and the importance of boundary conditions in determining carrier injection and ejection.

To understand switching to a high-current-carrying state, one needs to distinguish between this reproducible switching phenomena and a destructive mechanism that may finally lead to dielectric breakdown, arcing, and carbonization.

A microscopic picture of switching to a high-current-carrying state can be envisioned with the injection of free carriers from metal particles and their free flight through the thin dielectric material in between. Deep localized traps can capture mobile carriers, but this will have a minimum effect if the time of flight through the dielectric is much less than the time required by mobile charges to equilibrate with trap centers [12].

We argue that switching to a high-resistive state is an intrinsic property of a particulate composite where metal particles are embedded in an insulating matrix with a concentration close to the percolation threshold. We further claim that strongly localized defects in the insulator, surrounding the individual metal particles, form space charges that generate high electric fields in a direction opposing the current and inhibit charge flow. Injection and ejection of charge between the contact pads and the bulk of the epoxy are due to the presence of defects in the matrix layer on the ECF-563 epoxy preform surfaces.

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DEVELOPMENT OF A NEW METHOD TO EVALUATE THE WETTING BEHAVIOR OF SURFACE MOUNTED DEVICES

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Abstract

Recent progress in integration of electronic packages on the circuit-and component-level has lead to an increasing use of SMT (surface mount technology). Today, most SMDs (surface mounted devices) used in SMT are soldered by a reflow process. This soldering process requires a limited amount of solderpaste and a temperature profile to solder the components. To increase reliability of electronic packages and to reduce the failure-rate of manufacturing, it is important to inspect electronic devices before the soldering process. It is important to have good solderability of the connection areas in electronic devices to reduce processing defects. The presently applied solderability tests give information about the solderability of components only on the basis of parameters for wave soldering like a solder bath and a constant temperature. The transferability of this information to the reflow process is only partially given; therefore, a new method has been developed to investigate and classify solderability of SMDs in combination with solderpaste, substrate and a temperature profile. This computer-controlled method measures the wetting force and the time, under simulation of real processing conditions. With this experimental arrangement, the user can achieve information about the wetting behaviour of the “SMD - solderpaste - substrate - temperature profile” system. The processing capability of the components is investigated in a single, time- and cost-saving test set-up. It is not necessary to evaluate the solderability of the components by several stand-alone

experiments. This is significant for reflow soldering, since the newly-developed investigation method qualifies the solderability of components used in the reflow process in a single test, corresponding to real processing conditions. It makes it practical to test solderability of different types of SMD connections in combination with distinct solderpastes and temperature profiles. In addition, some experiments show the possibility to qualify solderpastes for the reflow soldering process. The aim to develop an experimental set-up which investigates the solderability of SMT components under conditions of the reflow soldering process has been achieved.

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AN INTRODUCTION TO SCANNING ACOUSTIC MICROSCOPY FOR ELECTRONIC MATERIALS EVALUATION

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The Assurance Technologies Division has recently procured a SONOSCAN C-Mode Scanning Acoustic Microscope (C-SAM) system. This article is a general description of a scanning acoustic microscope system to introduce its capabilities and applications for electronic materials evaluation. The fundamental principle of scanning acoustic microscopy is essentially simple: a high-frequency focused sound beam is transmitted and reflected (or transmitted through) from an object by using a diffraction limited single surface acoustic lens. An image of the object is constructed by scanning the lens (or the object) in a raster fashion.

The contrast of the acoustic image depends on the physical properties of the sample, acoustic impedance (product of density and speed of sound).

Typical Applications

1. high-resolution surface and near-surface imaging (<1 mm).
2. lower resolution subsurface imaging (>1 mm).

The greatest practical and economic benefits of acoustic microscopy lie in lower frequency range of 50 to 100 MHz. Although the surface resolution is above 10 mm, it is possible to image bonds at depths of up to several millimeters. The microacoustic imaging system is then able to reveal detail that is not discernible with any other techniques. Applications in the semiconductor industry are now widespread; a large number of bonds in transistor outline and integrated circuit packages have been examined.

Apart from the detection of bulk defects in the basic materials, the examination of bonded assemblies is one particular area where high-frequency ultrasonic probes are extremely valuable. Bonding of chips to substrate, heat sinks to substrate, lid seals, and silicon wafer assemblies are some examples, whether produced by eutectic or epoxy bonding, diffusion techniques, or soldering.

With the increasing use of surface-mount devices in populating circuit boards, the potential of SAM has been extended to the examination of soldered joints. A color C-scan can show the bond integrity of individual solder pads, spaced on a 1.25 mm grid, and the bridging of adjacent pads. Visual and radiographic examination may reveal bridging but would not show a partially made or detached joints.

Frequency (MHz)	Wavelength in Water (μm)	Resolution (surface)	Resolution in Material	Penetration (μm)
30	50	35	70-175	7000
50	30	20	40-100	5000
100	15	10	20-50	2000
500	3	2	4-10	40
1000	1.5	1	2-5	20
2000	.5	.5	1-3	10

DR. TAGUCHI VISITS JPL

by Charles J. Bodie
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Dr. Genichi Taguchi, the founder of Taguchi Methods of Robust Design, gave a lecture at California Institute of Technology on the morning of April 15. The session was hosted by the Caltech Industrial Relations Center. The attendance was formed by invited guests from industry, Caltech faculty members and students, and JPL personnel. The manager of the Avionic Systems and Technology Division, Garry Burdick, and a division technical staff engineer, Julian Blosiu extended the invitation to Dr. Taguchi to visit JPL for the afternoon of the same day. Dr. Taguchi graciously accepted the invitation to visit JPL and to listen to a summary of how JPL has used his methods in a number of space-related applications. Mr. Blosiu, who has studied the Taguchi techniques for a number of years and has been instrumental in the successful application of them in the solutions of several problems at JPL, presented a summary of the remarkable applications results of recent projects. He also touched briefly on the plans for the future use of Taguchi Methods in the development and qualification testing of advanced electronic packaging technologies, as well as other relevant space application technologies. Later, Dr. Taguchi remarked that he was impressed by the unique ways in which JPL had applied his methods.

In appreciation of Dr. Taguchi's participation in the afternoon session at JPL and to his contribution to the remarkable JPL results, he was presented with a composite photograph of each planet in the solar system which has been visited by NASA spacecraft.

ISWG INFORMATION EXCHANGE

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The Interconnection Standardization Working Group Information Exchange is provided as a service to project engineers NASA wide to keep them informed of issues in the commodities of fiber optics, connectors, wire and cable.

- The Connector Baseline: The EIA document entitled "Guide of Space Requirements for Electrical Connectors" has been approved for the pink ballot process. This is the final formal commenting process before the document becomes an American Standard. Contact me if you want to be added to the distribution listing. I will forward the information to my replacement.
- During the recent June 3-5 EIA meetings in Vancouver on interconnection Chair of the subcommittee on rectangular connectors was looking for interest in several specifications that are being developed by the subcommittee. If you have an interest in the following specifications please contact Doug Parker Chair of CE 2.3 at Glenair, 818-247-6000:
  - PN 3322, Blind-mate, Scoop-proof, Rectangular, Low Force, Subminiature, Electrical Connector for Space Flight Use.
  - PN 3323, Blind-mate, Scoop-proof, Rectangular, Low Force, Electrical Connector for Space Flight Use.
  - PN 3444, Rectangular Connector Standard for Spacecraft Interface Rack (SIR).
- There have been reports of Tefzel fiber optic cable jacketing shrinking in thermal-vacuum environments, and results in a microbend attenuation in the fiber. Rifocs Corporation preconditions the cable jacketing to eliminate this problem and will fabricate cable assemblies with your choice of fiber connector and cabling. You can contact Rifocs for more information at (805) 389-9800 and speak with Carrie Jaques.

SPACE REQUIREMENTS FOR HYBRID MICROCIRCUITS

S-311-200 D

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The GSFC Parts Branch recently published S-311-200, completely revising the document that specifies general requirements for hybrid microcircuits used in space flight hardware for compliance with MIL-PRF-38534. S-311-200 is not a procurement document though it gives detailed requirements and guidance information for testing and accepting hybrid devices. The intent is that projects use it as a guideline when writing source control drawings (SCD's) for new designs. It is not intended to apply to manufacturer's existing designs or SMD/QML product. The device specific SCD, while listing all design specific operational and performance data, can refer to S-311-200 to place specific restrictions and conditions on the processing and testing of flight parts. S-311-200 includes an appendix which instructs SCD authors about information that should be included, especially

information necessary to perform some of the qualification and screening tests, like burn-in biasing conditions and radiation exposure levels.

S-311-200 consists of a mix of "Class S" and "Class B" requirements to define one quality level. This specification not only covers testing requirements but also discusses product development from assessing the manufacturer's capability through packaging and delivery. Requirement paragraphs include Source Approval, Design and Construction, Process Control, Prototypes, Design Review, Element Evaluation, Screening, Quality Conformance Inspection, Marking and Serialization, Workmanship and Data Requirements. Much of information about implementing the tests and inspections conforms with MIL-PRF-38534 and MIL-STD-883. Some exceptions have been taken, such as changes to sample sizes and the elimination of redundant tests, to make the document more compatible with the "one time buy" environment common to most GSFC projects..

Copies of S-311-200, revision D can be obtained from Mr. John Bollman at the GSFC Office of Flight Assurance Library (john.r.bollman.1@gsfc.nasa.gov or 301-286-7240). Questions or comments about the document may be directed to Ms. Jeannette Plante at 301-286-9458 or jeannette.plante@gsfc.nasa.gov

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HITACHI EEPROMS

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High-density EEPROMs are being increasingly needed by NASA spaceflight projects. Previously, a number of NASA projects were using the 28C256 EEPROM, manufactured by Seeq. Total dose radiation testing of this part showed that failures could be expected in the range of 2.5 - 20 krads(Si). This part, however, has recently become unavailable, due to the manufacturer going out of business.

A 125K x 8 EEPROM has recently become available from Hitachi (Hitachi part number HN58C1001).The part can be purchased as a packaged part (32-pin plastic DIP and 32 lead Plastic SOP and TSOP packages) as well as in die form from Hitachi. Two packaging houses, Space Electronics Inc. (SEI) and Austin Semiconductor have packaged the die from Hitachi in their proprietary "Radiation Hard packages" . GSFC has performed total dose radiation characterization tests on these parts (SEI part number 28C010 and Austin part number AS58C1001). The radiation testing was performed using a Co-60 gamma-ray source. It should be noted that since gamma rays very effectively penetrate any parts package unlike the electrons and protons in the space environment , the test results presented below provide the radiation characteristics of the Hitachi die and not the shielding effectiveness of the radiation hard packaging by either SEI or Austin Semiconductor.

The dose rate during gamma ray testing was approximately 100 rads(Si)/hour. The radiation steps were 2.5, 5, 10, 15, 20, 25, 30, 50, 75 and 100 krads(Si). After the 100 krads(Si) exposure, parts were annealed for 384 hours at 25 °C , after which the parts were annealed for 168 hours at 100 °C. Initially and after each irradiation and annealing step, parts were tested according to the manufacturer's specifications. The parts were kept under static bias during irradiation and annealing.

Electrical parametric tests included power supply current, leakage current and output level, as well as AC timing measurements. The electrical measurements included nine initial (pre-rad) functional tests at 1.0 MHz: These functional tests were WRITE/READ ZEROES, WRITE/READ ONES and WRITE/READ CHECKERBOARD with Vcc = 4.75 V, Vil = 0.0 V and Vih = 4.75 V, the same three tests with Vcc = 5.00 V, Vil = 0.0 V and Vih = 5.00 V, and the same three tests with Vcc = 5.25 V, Vil = 0.0 V and Vih = 5.25 V. After the first (2.5 krad) irradiation, three additional functional tests were added. These were READ CHECKERBOARD tests, for the purpose of determining if the checkerboard pattern read into the parts before irradiation could still be read after irradiation. These tests were performed with Vcc = 4.75 V, Vil = 0.0 V and Vih = 4.75 V, with Vcc = 5.00 V, Vil = 0.0 V and Vih = 5.00 V and with Vcc = 5.25 V, Vil = 0.0 V and Vih = 5.25 V.

All irradiated parts (four from SEI and three from Austin) passed all functional and electrical parametric tests up to and including the 50 krad(Si) level.

The SEI parts passed functional tests up to 100 krads(Si), however, the Austin parts failed functionally at 75 and 100 krads(Si). After annealing for 384 hours at 25°C, two of the three Austin parts passed all functional tests, while one part continued to fail functionally.

Both Austin and SEI parts passed all parametric tests up to 20 krads(Si) and were within the specification limits provided by the manufacturers. However, at 30 krads(Si) and above, some degradation in both ICC and IIL was observed in the Austin parts, while the SEI parts showed degradation only in IIL. The ICC readings for the SEI parts ranged from about 22 to 30 μA, against a specification limit of 20 μA. The IIL readings for both SEI and Austin parts ranged from 8 to 50 μA at the 100 krads(Si) level, against a specification limit of 2 μA.

On annealing the parts at 25°C up to 384 hours, some recovery was observed for both parameters. No rebound effects were observed on annealing the parts for 240 hours at 100°C.

Details of the radiation test data can be obtained by calling the GSFC Office of Mission Assurance Information Center,

John Bollman, 301-286-7240, or
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and citing the report numbers, PPM-95-182 and PPM-96-003 for the SEI and Austin parts, respectively.

ASAP CORE SUPPLIERS LIST, PART II

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Core Supplier List (CSL) Part I was released on November 27, 1995. This CSL Part I listed QML 38335/ QPL 38510/ QPL19500 suppliers with one or more products listed in MIL-STD-975 or GSFC PPL. The CSL Part II is a supplement to CSL Part I and contains microcircuit and semiconductor suppliers who satisfy one or more of the following criteria:

- Manufacture parts on a DESC certified and qualified line,

- Have compiled a satisfactory history of supplying high reliability parts which are currently procured through contractor (or OEM) SCDs,

- Have high NASA usage parts available to approved NASA specifications and

- Are certified and qualified by European Space Agency (ESA) or National Space Development Agency of Japan (NASDA) to provide parts to ESA/ Space Components Coordination (SCC) or NASDA specifications.

ESA: The Space Components Coordination Group (SCCG), composed of space components experts, is in charge of managing the ESA/SCC system. The group reviews and monitors the qualifications, extension of qualification and renewal of qualification program. The SCCG Secretariat is located at:

European Space Research and Technology Center
(ESTEC)
P.O. Box 299
NL-2200 AG
Noordwijk, The Netherlands

NASDA: The NASDA EEE (Electrical, Electronic, and Electromechanical) Parts Program Standard establishes selection criteria, standardization procedure and control of EEE parts. The NASDA qualified parts are commonly used in Japanese space systems which are developed by NASDA. The Agency is located at :

2-4-1 Hamamatsu-cho
Minato-Ku
Tokyo, Japan

For each manufacturer described in the CSL Part II there is accompanying information related to the processing technologies, product types, certified /qualified facilities, package information, and part listings for which the manufacturer is considered a core supplier. This CSL Part II Draft is currently under review with other NASA Centers and ESA/NASDA suppliers. This document will also include NASA high usage suppliers/ parts being used on various NASA programs such as ISTP/ GGS, NOAA, GOES, EOS, CASSINI, SPACE STATION, etc. A final copy of this document is expected to be released by mid-September 1996. For further information, please contact: Ashok Sharma at 301-286-6165 or Nick Virmani at 301-286-6916.

REPUBLIC ELECTRONICS CORPORATION REMOVED FROM QPL FOR MILITARY CAPACITORS

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In February 1996 Republic Electronics Corporation of Wilkes-Barre, PA requested removal from the Qualified Products List (QPL) for MIL-C-20, MIL-C-55681 and MIL-C-11015 ceramic capacitors. In April the Defense Electronics Supply Center (DESC) officially removed Republic from these QPLs. This action has created a situation where there will be no qualified source for certain part types such as the CDR26, 27, 28, 29, and 30 high voltage ceramic chips of MIL-C-55681/6.

A November 1994 DESC audit of Republic and subsequent investigations found numerous deficiencies which lead to a suspension of shipments for all of the above military part types. Republic has been unable to make the corrective actions necessary to remain on the QPL and has opted to relinquish their qualification status. Republic has the option to reseek qualification, but this would require them to make appropriate corrective actions and begin the lengthy qualification process from the beginning.

AN ADVANCED ULTRASONIC SYSTEM FOR DEFECT IMAGE ENHANCEMENT

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A paper entitled "An Advanced Ultrasonic System for Defect Image Enhancement was selected for oral presentation at the First US-Japan Symposium on Advances in NDT held on June 25-28, 1996. The following is the abstract:

Typical ultrasonic C-scan images are two-dimensional pictures with false-color palette or grayscale shades representing signal magnitudes on an X-Y plane. Amplitude images provide proportional reflected signal strength data while Time-Of-Flight (TOF) images provide information related to time intervals between the start and stop pulses. However, interpretation and correlation of false-color or grayscale coded 2-D amplitude and/or TOF images may be difficult. Processing algorithms are necessary to interpret geometry signals and to convert time information into depth information. We have developed an advanced ultrasonic C-scan imaging system that enables the acquisition of multiple TOF and amplitude data, and the merging of ultrasonic amplitude and processed TOF data in a composite C-scan image. This composite image provides an enhanced pseudo 3-D display of detected defects. The composite image is comprehensive and does not require ultrasonic specialists to interpret. In this paper, we will review the principle of operation, describe hardware configuration, outline software requirement, and present experimental verification. The results provide improved visualization of defects for enhanced ultrasonic C-scan imaging.

TEST RESULTS AND ANALYSIS OF POST PROGRAMMING PROM BURN-IN FAILURES ON NOAA PROJECT

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Introduction:
Two Harris microcircuits (HS1-6617RH-Q, S/N 21 and 24) being used by the NOAA project were submitted to the GSFC Parts Analysis Lab for failure analysis by Panametrics Corporation. They were from a group of 12 devices which failed post programming burn-in and electrical verification testing at Assurance Technology Corp. Three of the 12 devices failed program verification during programming, and the rest failed during post burn-in electrical test. In addition, S/N 21 failed parametric electrical testing following dynamic burn-in.

Evaluation Test plan:
An evaluation test plan was developed to simulate the program verification failures on NOAA parts. One of the probable causes of failure is leaving the pin P (Program Enable) floating, instead of hardwiring it to VDD during all phases of testing, as recommended by the manufacturer's data sheet. Therefore, the program was developed to subject the parts to various phases of testing using two different batches - one with pin P floating, and the other with pin P hardwired to VDD. To assist this evaluation, twenty parts (HS9-6617RH) were provided as "sacrificial" samples from a project unused residual lot, in order to identify factors in the screening process which could cause these types of failure. It should be noted that similar failures with HS1-6617RH-8 devices had occurred during the post programming burn-in and electrical measurements for POLAR/MFE project at Qualified Parts Laboratory (QPL), Sunnyvale, CA.

A brief summary of the test results is provided below. For detailed information refer to report number FA51708, October 10, 1995.

NOAA Parts Failure Analysis Results:
External visual and radiographic examinations on two parts HS1-6617RH-Q (S/N 21 and 24) revealed no defects. The devices passed PIND and fine leak hermeticity testing. Data-read verification tests were then performed at a temperature of +25 degrees C on the Sentry S-50 tester, using patterns provided by Panametrics. Supply voltages were varied between 4.50 and 5.50 volts, and operating frequency was varied between 1.00 and 6.25 MHz. The results confirmed failures of the parts and revealed incorrect data bits at several addresses. The parts

were then de-lidded, and inspected with a high-power (200X) optical microscope. No defects were found.

After glassivation removal by etching, the parts were examined using a scanning electron microscope (SEM). The fuses mostly had the appearance of a typical "one" or "zero"; clearly blown or unblown. However, some of the fuses were blown only slightly and their appearance did not suggest a clear "one" state had been accomplished. SEM bit-map reading was found mostly to confirm the electrical test data. With 26 bits expected to be "1", and electrically tested as "1", only one (4 %) was found to be marginally blown. The proportion of marginally blown bits among the bits expected to be "0", but electrically tested as "1", was much higher 48% (13 out of 27). The failed fuses were probably blown by less powerful pulses than the fuses which were properly blown during programming.

Failure "Simulation" Testing Results:

Table 1 shows the test results for failure simulation testing. Three groups of samples (S/N 1-5, 6-10, and 11-15) were tested with pin P floating. The results are as follows:

1. Program verification with pin P floating (step 3) for S/Ns 1-5 indicated 5 failures. However, additional testing showed these 5 failures to be invalid, since the program verification on DATA I/O Programmer cannot be performed with pin P floating (open).

2. Electrical measurements of S/N 6-10 with pin P floating (step 5) indicated that all samples failed. However, additional verification testing (step 6) showed only 4 failures out of 5 as being valid (i.e., the result of leaving pin P floating).

3. Post dynamic burn-in electrical testing of 5 devices out of 20 that were subjected to burn-in with pin P floating showed 4 failures in addition to 4 earlier device failures confirmed (steps 5 and 6). A total of 8 failures had occurred during screening sequence steps 5-8, as a result of leaving pin P floating. The failure mode is a change of bit pattern as compared to the original program pattern. No failures were observed during this screening sequence for parts with pin P hardwired to V_{DD}.

Table 1. Electrical test results of HS9-6617RH.

Step	Test	QTY tested	QTY failed	Comments
1	Initial electrical measurements	20	0	
2	Programming	20	0	
3	Program verification S/Ns 1-5 with pin P floating	20	5	The failures were not confirmed when the samples were tested with pin P hardwired to VDD.
3a	Program verification with pin P with pin P hardwired to VDD	20	0	
4	Electrical measurements	20	0	
5	Electrical measurements S/N 6-10 with P pin floating	5	5	The failure indication may be be due to P pin floating
6	Electrical measurements retesting S/Ns 6-10 with P hardwired to VDD	5	4	Only S/Ns 6,7 and 9 failures confirmed.
7	Dynamic burn-in. S/Ns 11-15 with P pin floating	20	0	
8	Electrical measurements with P pin hardwired to VDD	20	8	S/Ns 11,13,14, & 15 failed. S/Ns 6,7,9,& 10 failed as before.
9	Electrical measurements after ESD tolerance test.	3	2	S/Ns 18 and 19 failed

One sample of each of the three groups, which were tested with pin P floating (S/N 2, 9, and 11) was de-lidded, and inspected with a high-power (200X) optical microscope. No defects were found.

SEM examination to verify bit-map data was performed after glassivation removal by etching. For S/N 2, a consistency was observed between the electrical test data, SEM data, and expected data. A fuse misalignment relative to aluminum contacts was found in S/N 2. This could have caused an increase of the fuse resistance. S/N 9 and 11 had fuses which were partially blown, and their appearance did not suggest that a logic "one" state had been accomplished. Due to the large proportion of marginally blown fuses, SEM bit-map reading failed to confirm the electrical test data or expected data. With 29 bits expected to be "1" and electrically tested as "1", six (21 %) were found to be marginally blown. The proportion of the marginally blown bits among the bits expected to be "0", but electrically tested as "1" was higher, 61% (11 out of 18). This suggested that the failed fuses were probably blown by less powerful pulses than the fuses which were successfully blown during programming.

Electrostatic Discharge (ESD) simulation was then performed with an Electrostatic discharge sensitivity test system in accordance with MIL-STD-883C, Method 3015.4, using the human body model (HBM, 100 pF and 1500 Ohms). The ESD tester was charged at 2 kV (with ±15 V tolerance). Five pulses with a 1 second delay between pulses were applied first between each non-supply pin and all other non-supply pins connected together; then between each non-supply pin and VDD and GND connected together; and then between VDD and GND. For each combination of pins, pulses of positive polarity were first applied and then pulses of negative polarity. Three samples (S/N 18, 19, and 20) were subjected to ESD simulation and then tested on the Sentry S-50. During the programming process, the VDD voltage was increased up to 10 V and current up to 500 mA. With a programming pulse width of 100 ms, the energy generated in a fuse causing it to be blown was approximately $5x10^{-4}$ joules. ESD simulation at 2 kV and pulse width of approximately 150 ns would have generated a similar quantity of energy ($4x10^{-4}$ joules) This means that one could have expected fuses to be blown after a 2 kV ESD event. Electrical measurements revealed two failures (S/N 18 and 19). S/N 18 failed functional testing with multiple (more than 100) incorrect data readings. Both samples had parameters out of the specification limits. All data pins (except Q0 and Q4) had excessive leakage current, which probably resulted in an approximately 4% increase of the operating supply current (IDDOP). One data pin (Q4), two address pins (A1 and A10), and chip enable pin (E) were damaged in S/N 19 resulting in a leakage current increase. S/N 20 passed functional and parametric tests. S/N 18 and 19 were then de-lidded and inspected with a high-power (500X) optical microscope. No defects were found.

SEM examination was performed on S/N 18 after glassivation removal by etching to find defects caused by the ESD simulation. No damage was detected in circuitry in the vicinity of the data pins. As previously reported, 48% of the fuses were found to be marginally blown (22 out of 48 inspected). A fairly good consistency between the expected data and SEM examination was revealed. This suggests that the ESD damage did not result in a blown fuse. The functional test failure was probably due to some hidden damage to the address decoder after 2 kV ESD testing. After 2 kV ESD testing, the most likely failure was caused by the damaged coder circuitry rather than the fuse blowing.

Conclusions:

The failures of the Harris HS1-6617RH-Q PROMs, S/N 21 and 24, were confirmed. Electrical testing and SEM examinations showed the bit pattern to be different from the expected (initially programmed) pattern. Also, inadvertently programmed zeros (blown fuses) were found but no site of "healing" of a blown fuse was detected. It was observed that approximately half of the bits, which were expected to be "zeros" but electrically tested as "ones", were marginally blown. The failures were probably due to a low power pulse (as compared to the programming pulse) occurring during screening irregularities such as leaving the programming enable pin P floating. Simulation testing of "sacrificial" HS9-6617RH samples for failed bits showed that program verification at the DATA I/O with pin P floating did not cause any failure. The failures occurred after electrical measurement at the Sentry S-50 with pin P floating and after burn-in testing with pin P floating. In both cases, the failed memory devices' bit pattern readout was different from the initially programmed pattern, i.e., the failures were similar to those which occurred at the test laboratory. All incorrect bits were "ones", which were expected to be "zeros". Most of them (61%) were marginally blown, suggesting that a low power pulse could have caused this failure mode. An ESD simulation was performed with voltage of 2 kV in accordance with MIL-STD-883C, Method 3015.4, using the human body model (HBM, 100 pF and 1500 Ohms). Two samples out of three failed, which implies that the parts do not conform to "Class 2" of the ESD specifications. One sample failed functional testing with multiple wrong data readings. Both samples had parameters out of the specification limits. SEM examination after glassivation removal revealed no visible defects caused by the ESD simulation. The bit map verification testing showed a fairly good consistency between the expected data and SEM examination. The results suggest that the ESD effect probably did not cause blown fuses.

Recommendations:
Post programming burn-in failure and simulation testing has shown that bit failures can occur in Harris HS6617 PROMs. These devices are particularly susceptible if pin P is left floating during screening sequences, such as automated equipment (ATE) electrical testing, as well as burn-in fixturing and post electrical verification. Therefore, post programming burn-in on these PROMs is not recommended, unless performed under carefully monitored conditions to assure that programming pin P is hard-wired to VDD (as specified in the Harris data sheets) during all phases of screening and testing. For additional details and SEM pictures contact the GSFC Office of Flight Assurance library 301-286-7240 and ask for report number FA62327.

If immediate assistance is required, please contact Ashok Sharma at the number or email address listed above.

QUALIFICATION OF RAD HARD OXIDE-NITRIDE-OXIDE (ONO) ANTIFUSE FPGA (RH 1280)

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This summarizes the key areas and activities that were reviewed by GSFC along with DESC-ELSC for QML marking of rad hard FPGA (RH 1280). Loral Federal Systems, Manassas (LFSM) and Actel Corporation has jointly developed a space qualified radiation hardened Field Programmable Gate Array (FPGA) (manufactured by Loral Federal Systems, Manassas and marketed by Actel Corporation). The prominent task to implement rad hard FPGA at LFSM included the transfer of Actel's design of existing circuits/devices, the integration of Actel's ONO antifuse technology into LFSM's existing QML qualified rad hard process and the performance to achieve QML qualification. Key radiation hardened FPGA process features are:

- Antifuse elements built before the transistors to minimize any effects of transistor parameters.
- Lower field doping and increased field oxide thickness to increase junction breakdowns while maintaining high field threshold voltages.
- Modified retrograde n-well in thicker EPI for high breakdown voltages while maintaining radiation hardness.
- Thicker gate oxide and lightly doped drain/source for high voltage transistor to route high programming voltage while maintaining high performance on normal low voltage transistor.
- All other features including the planarized back end of the line process are identical to RHCMOS-E process.

QML qualification data review and approval included product functionality, necessary screening and testing to group A, B, C, D and E and establishing of manufacturing process for achieving QML qualification. FPGAs met the radiation testing requirements of total dose of 300 K Rad. The following is the product radiation summary:

ENVIRONMENT	RADIATION LEVEL
Total Dose-Gamma Cobalt 60	300 K Rad Full Range
SEE's:	
- Single Event Gate Dielectric Rupture	<< 1 FIT
- SEU Heavy Ions	IE-06
- SEU Protons	Sensitive
- Latch Up	Immune
Dose Rate	> 1E+09 Rads/s Full Range
Survivability	>1E + 12 Rads/Full Range (projection)

FPGA (RH 1280) will be included in core supplier list part II as an approved product for NASA usage. This product is now available as QML SMD part no. 5962F9215603VYC through Actel .

For additional information please contact Ashok Sharma at 301-286-6165 or Nick Virmani at 301-286-6916.

TOTAL DOSE RADIATION TESTING FOR GODDARD PROJECTS

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Total dose radiation testing of spacecraft parts at GSFC is performed in the range of 0.01 -0.5 rads(Si)/sec., which is fairly low, compared to the dose rate range of 5 -300 rads(Si)/sec, commonly used by manufacturers, as well as other test laboratories. This low dose rate testing at GSFC allows us to better simulate the effects of the space radiation environment. The table below provides a listing of parts tested for total dose radiation effects at GSFC during the period October, 1995 - May, 1996.

Part Type	Manufacturer	Project	LDC	Report #
Op Amp	Analog Devices	HST/NICMOS	9435	PPM-95-183
DAC	Analog Devices	HST/ADD	9449	PPM-95-176
EEPROM	SEI/Hitachi	AXAF/Gulton	9530	PPM-95-182
DAC, 18-bit	Sipex	XDS/ACHE	9509	PPM-95-184
DAC, 8-bit	PMI/Analog Devices	CASSINI/CIRS	9435	PPM-95-185
CMOS SRAM	Micron Tech.	AXAF/Gulton	9421 9515	PPM-95-186
EEPROM	SEI	AXAF/Gulton	9543	PPM-95-187
EEPROM	Hitachi/Austin	GPEP-PPL	-	PPM-96-003
DC/DC Conv.	Interpoint	CASSINI/CIRS	9603	PPM-96-004
FPGA	Actel	HST/FLEX/HSR/SSR HST/SSR	9607 9541	PPM-96-005
NPN transistor	unknown	MASUNI040896	Lot #9402C101-5	PPM-96-006
Quad 4-input NAND	unknown	MASUNI040896	Lot #0131001-35	PPM-96-007

NOTE: Radiation results vary significantly with the Lot Date Code (LDC) and any variation in the process technology by the manufacturer, as well as with details of the radiation testing, such as dose rate, bias conditions, electrical parameters and functional characteristics measured. The information in these reports is for general guidance only, and is subject to change at any time. Qualified users may obtain a copy of Goddard radiation test data on any part type listed in Table I by submitting a request through their project office to the Office of Mission Assurance (OMA) Information Center, Code 300.1, NASA/Goddard Space Flight Center, Greenbelt, MD 20771. (301) 286-7240. Please cite the PPM report number in your request

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SOLDER JOINT FAILURE INSTRUMENTATION FOR TESTING BALL GRID ARRAY ASSEMBLIES

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BACKGROUND- JPL, in partnership with an industrial consortium, is engaged in the investigation of reliability and quality issues of Ball Grid Array Packages as they may be applied to space flight electronics. This effort is funded in part by a Code Q RTOP with the industry partners contributing from their IRAD funds. JPL is the lead in this consortium with the others supplying parts, assembly labor, printed wiring boards, and design of the test printed wiring boards. JPL is also performing a significant portion of the laboratory tests on the samples to determine the reliability of the interconnections of the BGA packages to the Printed Wiring Boards (solder joints).

APPROACH- It was recognized early in the program that a large number of the BGA solder joints would be under test simultaneously and that some sort of computer based assistance would be required to accurately track the failures and the time at which they occurred. The test plan called for over 1500 channels of data each representing up to 150 solder joints to be monitored 24 hours a day for several months of temperature cycling . (At the time, the

test capacity at JPL was approximately one-tenth of this requirement.) A failure of any channel when detected was not only to be identified to the card and channel, but also to be annotated with real time, temperature at the time of failure, and the total number of temperature cycles experienced by the particular channel from start to failure. However, it also was recognized that the purpose of the RTOP funds was primarily to investigate Ball Grid Array interconnects and not to develop test instrumentation. Therefore, the approach adapted was to use off-the-shelf hardware and software and to minimize development. This approach was ,in the main, quite successful, but some development, particularly in the software arena was found to be necessary.

JPL has been using the National Instruments LabVIEW™ software and has collectively a great deal of experience in its application to laboratory testing. National Instruments also offers a suite of hardware which compliments the software operating system. As an added attraction to the RTOP team, the JPL equipment loan pool owned sufficient inventory of software and hardware so that the project could rent and return it at the end of the study again minimizing the costs to the RTOP.

DETAIL DESCRIPTION. The data acquisition system program, DAQ.VI, was written around the LabVIEW graphics-based operating system and using the hardware handlers provided by National Instruments. The program controls the temperature chambers, gathers the data from the interface cards, logs the data onto a spread sheet type data base, and provides operator interface for ease of operation. Figure 1 is a block diagram of the laboratory test system.

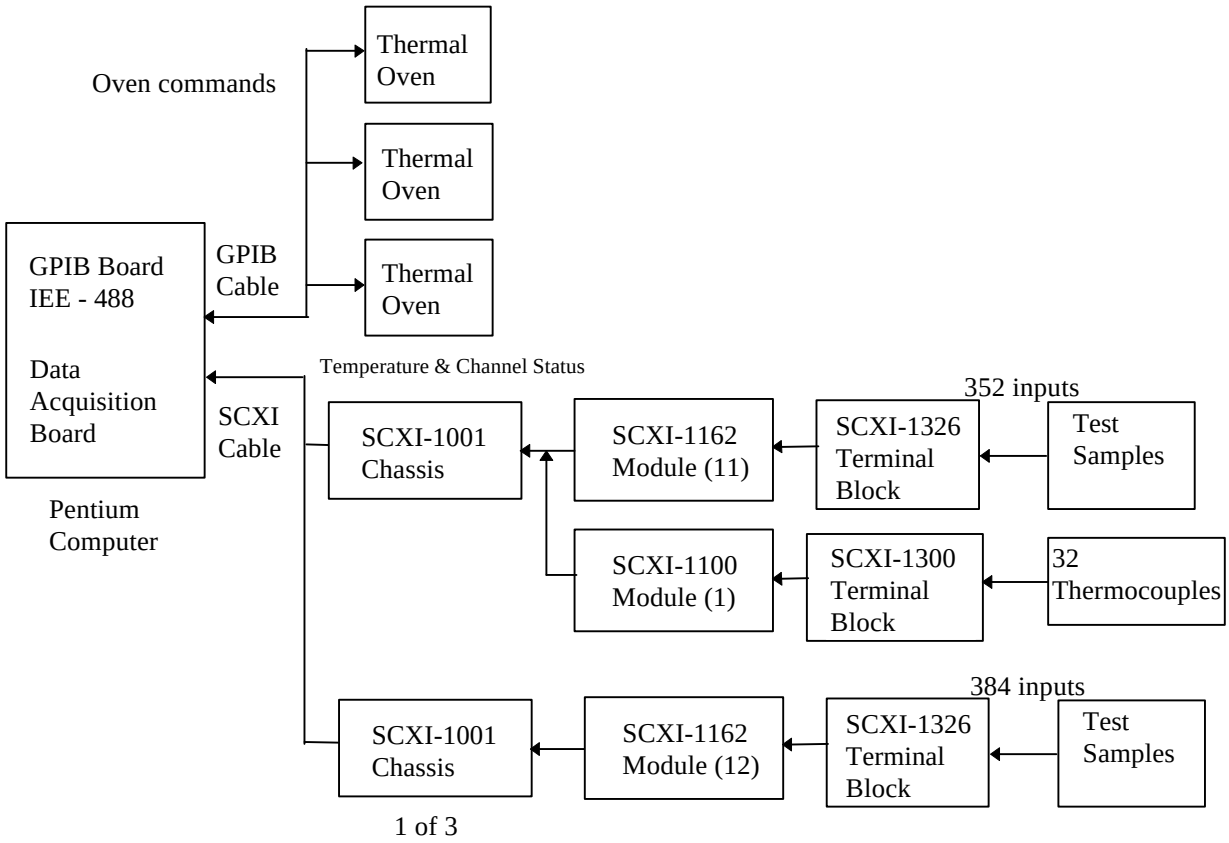

Figure 1. Test Instrumentation Block Diagram

The software is installed in a Pentium Personal Computer which also contains a Nation Instruments IEEE-488 General Purpose Interface Board and a special Data Acquisition (DAQ) Board Model AT-MIO-16E-10 also supplied by National Instruments. Connected to the GPIB board are three Thermotron thermal chambers. This IEEE bus can be expanded to control other devices such as power supplies for the cycling of heating elements mounted on the BGA devices to simulate the heat that active devices would normally dissipate.

The DAQ board is connected to National Instruments SCXI hardware interface modules installed in 4 National Instruments card cages. The SCXI hardware consists of 4 SCXI-1001 12 card chassis, 47 SCXI-1162 discrete input modules, and 1 SCXI-1100 thermocouple input module for a total capacity of 1503 discrete inputs and 32 temperature inputs.

The Discrete Input module (SCXI-1162) is a 32 channel device with optical input coupling. Input isolation provided by the optical coupler front end of this module was considered to be a prerequisite because of severe ground loop noise problems encountered with other instrumentation schemes that had been used in the test laboratory. The relatively low input impedance of the front end , 360 ohms, also helps fight the electrical noise inherent in the environment of the test facility. Figure 2 is a block diagram of the input stage of the module. The BGA packages are wire bonded internally so that when combined with the circuitry on the test PWB, a daisy chain of up to 150 solder joints is formed. Each discrete input channel monitors one such daisy chain by detecting the presence or absence of approximately 7 milliamps of current through the LED portion of the optical coupler device.

The thermocouple module provides 32 channels of input which provides for the measurement of local temperatures (i.e. in the vicinity of the test samples).

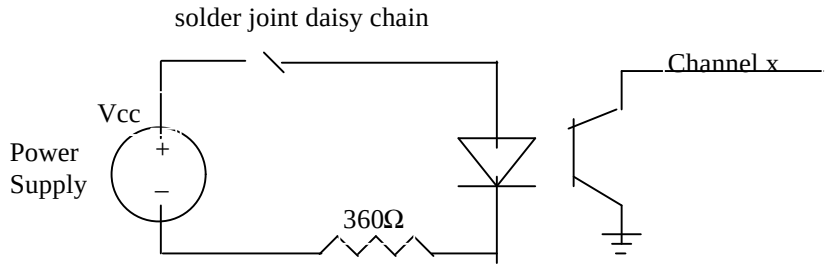

Figure 2. Input Block Diagram

When a solder joint breaks, the current will not be able to pass through the solder joint, so the LED will not get the current it needs to light. When the LED is turned off, the light-sensitive transistor sends back a logic high to the computer telling the computer that something is wrong with the channel. The computer reads the logic high and knows that a solder joint has failed.

The DAQ.VI program will display an event (a circuit either opening or closing), along with a message that shows the channel number, test board number, board location, time, cycle number, date, and temperature that the event occurred. Figure 3 is a depiction of the operator interface displayed on the computer monitor. It was deemed important to record both openings and closing of the circuit to detect intermittents if they occur.

This information is also written to a file that can be brought up in a spreadsheet program. DAQ.VI also keeps track of the number of thermal cycles each board accumulates, the board location, serial number, and its corresponding channels (16 per board).

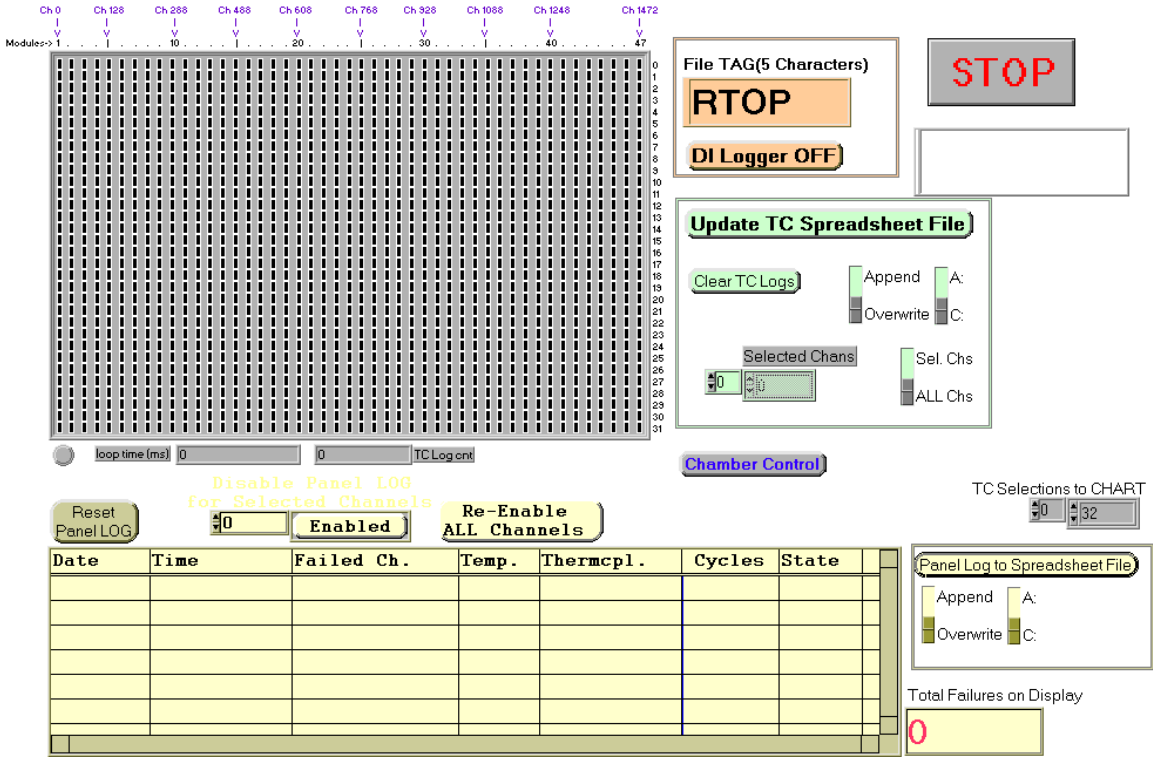

Figure 3. Operator Interface Display

Conclusion- JPL has developed an instrumentation system for the testing of solder joint reliability and longevity. This software/hardware system greatly simplifies the task of monitoring and tracking failures and the conditions when the failures occurred of a large number of solder joint channels through the automatic gathering and recording of the test results onto a personal computer data base.

BIPOLAR TRANSISTORS AND TOTAL DOSE HARDNESS

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In a recent meeting, Dr. Ronald Schrimpf of the University of Arizona made the following comment concerning the total dose hardness of bipolar transistors and has allowed me to gratefully relay it.

In essence, PNP transistors tend to be less susceptible to total dose than NPN transistors. Additionally, complementary vertical PNP transistors appear to be better (more tolerant to total dose) than lateral PNP transistors. This information is to be used as a rule of thumb. Specific devices might react differently, but as a first rule for designers creating a parts list, it is a good step.

PROGRAMMABLE LOGIC APPLICATION NOTES

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This column will be provided each quarter as a source for reliability, radiation results, NASA capabilities, and other information on programmable logic devices and related applications. This quarter the focus was to be on radiation-hardened PALs; however, because of time constraints, that has been postponed to the next issue. This issue will focus on results of testing the RH1280 and other manufacturers FPGAs as well as some more design tips. Many of these tips are based on actual failures in the field at various NASA and industry sites and are fairly common. If you have information that you would like to submit or an area you would like discussed or researched, please give me a call or an e-mail.

DESIGN TIPS

CLOCK SKEW: Failure to properly manage clock skew is a major source of failures in FPGA designs. There have been a number of instances where 'proven' designs have failed when the flight devices were installed into 'working systems' or intermittents would be eliminated by re-routing a device. The causes of these failures was twofold: improper understanding of clock skew inside FPGAs and models which did not accurately reflect delays within the device.

The Actel anti-fuse based FPGAs provide high-speed, low-skew global and quadrant clocks. There is one global clock for the 1020 devices, 2 global clocks for the 1280's, 3 global clocks for the 1460/14100's (two routed, 1 dedicated), and up to 6 clocks (two global, 4 quadrant) in some models of the A3200DX family. For the Act 1 A1020x devices, the user can instruct the placement and routing software how much effort to expend on clock balancing, trading off clock skew for system performance. The other series devices have improved clock networks where this is not necessary. So, by appropriate 'balancing' in the Act 1 family and normal usage of the global clocks in the other devices, clock skew is normally not a problem. Adequate timing margins can easily be calculated using TIMER.

When regular signals are used as clocks, care must be taken to ensure that setup and hold times are guaranteed to be met. Routing clock signals inside of an FPGA is not the same as routing a clock on a printed circuit board (PCB). Signal propagation delay is often negligible on a PCB and is frequently neglected as a major source of clock skew. However, for example, proper clocking is sometimes difficult when using CD40xxB logic where clock signals may have long transition times and flip-flops can have threshold varying from 30% to 70% of V_{DD}. This can result in the parallel clocking problem where hold times may not be met since the data to the flip-flop may change prior to the clock signal reaching the logic thresholds. Since signals routed in an FPGA must propagate through a number of segments and antifuses, the arrival of the clock at various points on a network will not occur at the same time. This results in clock skew and an equivalent problem to the CD40xxB parallel clocking problem.

Certain structures are extremely sensitive to this. For example, shift registers, which have little or no logic between stages, are very prone to failure. A change in either supply voltage or temperature can cause problems to appear and disappear. In general, any structure that employs parallel clocking needs to be carefully looked at. Also, soft macros *appear* to have a common clock input. They don't. It is a *soft* macro and the clock will propagate down a clock tree with skew between the leaves if not on a low-skew clock bus. So, easy to use macros like the TA161 counter or macros generated by ACTGen which are guaranteed to be correct by construction can fail if improperly clocked although they appear fine on the schematic.

Compounding this problem are the models used to simulate the designs. At two different contractors these issues were explored in depth to analyze their failing systems with both groups performing full simulations. However, they used a logic simulator to perform their timing analysis and either didn't use or improperly used TIMER. In both cases, however, the logic simulator did not model the clock skew between flip-flops, assumed all clocks arrived at the same time, and 'passed' the circuits.

There are a number of different solutions to these types of problems and some will be briefly discussed here. First, if the design can be made synchronous, use the global clocks. The hard macros supplied by Actel minimize the pain caused by the architectural limitation of a small number of low-skew clocks. These macros include flip-flops with enables and flip-flops with multiplexors on the inputs. Another approach is to utilize a structure where flip-flops that communicate pass data between opposite edges of the clock. This moves a clock skew problem into a clock width consideration and possibly a device utilization issue. A more compact solution but with more complexity is to use a two-phase non-overlapping clock structure with one-module latches. Another technique is, where possible, to eliminate the use of synchronous counters and use ripple counters or a hybrid counter where the first stage is synchronous which feeds the remaining stages that operate in a ripple mode.

CALCULATING PROPAGATION DELAYS FOR ACTEL FPGAs: Calculating propagation delays with a static timing analyzer like TIMER is critical for ensuring that there are no races, setup and hold times are met, etc. Now, with TIMER, it is quite easy to determine minimum and maximum delays for sets of paths. However, it should be noted that in certain cases the minimum numbers reported by TIMER need to be 'adjusted.' The calculations done for the minimums are not worst-case minimums and may in fact be longer than the actual delays. So, for minimum paths, a derating factor must be applied. These can be found in the 1995 Actel Data Book on page 10-57 in an application note titled "Setup and Hold Time Analysis Using the Actel Timer." Also included in this note is useful equations for determining the parameters. For example, the derating for a A1020 would be 0.7 for all paths. For the A1280A, there is a 0.78 derating for all combinatorial paths and a 0.85 derating for the routed global clock.

PERFORMANCE COMPARISON BETWEEN VARIOUS FAMILIES: A reference test design was implemented in three different technologies for performance comparisons. The same data base was used for all designs with no placement or routing changes. Additionally, common 'environmental' conditions were used. These are: pre-rad, V_{CC}=4.5VDC, standard speed grade, worst-case process, and a junction temperature of 85°C. The three devices simulated were the A1280A, the A1280XL (0.6 µm), and the RH1280. As can be seen from the table below, there are significant overall speed differences. One comes from the technology as seen in the Reg -> Reg delays and a more significant increase in performance comes from the I/O cells as shown by the I/O performance. All data is in nanoseconds in a min/max format. The simulations were performed using Designer 3.0.1s on a PC.

	INPAD -> REG	REG -> REG	REG -> OUTPAD
A1280A	10.5/25.1	6.3/36.3	8.8/84.8
A1280XL	6.2/15.5	4.1/30.4	4.3/64.1
RH1280	5.0/13.6	3.6/24.3	3.6/51.9

PIN ASSIGNMENT ERRATA: In the 1994 data book Military Section, there is an incorrect pin assignment for the A1280A CPGA176 package. The letter sequence calls out ABCDEFGHJKMNPQR. It should be ABCDEFGHJKLMNPR.

UNUSED INPUTS: The termination requirement for unused inputs was addressed in the October 1995 issue of EEE Links. One design that was reviewed treated the unused pins of the A1020 devices like inputs of a regular CMOS device and tied all pads on the PCB for unused pins to GND. Now, since the unused pins are configured as either outputs driving low or as high impedance, this seems to be *logically* fine. However, upon the application of power, pins may act as outputs driving high and can source considerable current. So, along with the startup current transient associated with the Actel devices, current will be sourced to ground through these unused pins as the device starts and stabilizes [see "A Power-On Reset (POR) Circuit for Actel Devices].

HIGH LEVEL DESIGN: High level design methodology is growing in popularity. However, it is strongly recommended that the design flow include schematic generation for any synthesized or optimized blocks. This aids in the communication with tools for static timing analysis, for instance, as well as troubleshooting. Also, the tools may do something considerably different than the designer anticipates, with an impact on proper operation of the device and timing margins, particularly for asynchronous circuits.

PRESETS and CLEARS: For discrete parts such as the standard 54LS74A, it has been observed that some designers assert both the PRESET and CLEAR simultaneously. Some sequential macros, such as the DFPC, have the capability for asserting both of these asynchronous inputs. While the 54LS74A guarantees that the output of the device will be a logic '1', tests on an A1020B showed that asserting both the PRESET and CLEAR of the DFPC resulted in a high frequency oscillation of approximately 150 MHz!

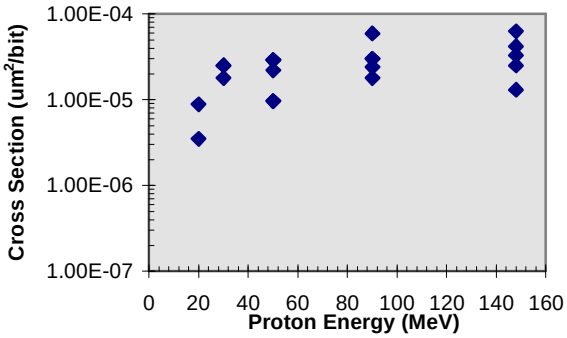
DESIGNER 3.0 COMBINER: In Designer 3.0, the default behavior of the combiner function has been changed from earlier versions and a description of the current operation of this software is given in Actel's User Guide. While the goal of the Combiner is to give faster, denser, more routable designs, this may impact circuit performance. For instance, a string of buffers inserted to create a delay (ugly, but sometimes needed) will be collapsed into a single element which is *logically* equivalent. However, if the delay is needed to create adequate set up times for an external signal interface, for example, the macros will be deleted without warning. This will be detectable, however, when running the static timing analyzer TIMER. Also note that there is a bug in the generation of the .cob file where deleted macros are not always recorded. To instruct the combiner not to perform this function, attach the attribute 'PRESERVE' to the net being driven by the macro that is desired not to be collapsed.

SEE PERFORMANCE OF FPGAs

As discussed, flight applications of FPGAs are increasing with more designers starting to utilize these devices. In the commercial/military marketplaces devices with new architectures and increasing performance and density levels are constantly appearing. A variety of NASA and industry groups are involved in the testing and evaluation of these devices. Recent tests include the RH1280, A1280XL 0.8 µm, A1280A, A1460A, Quicklogic FPGAs, Atmel AT6002, Xilinx XC3090A, and the AT&T ATT2C04-2. For SRAM-based FPGA's, along with typical data upsets, the configuration of the part may be changed by an SEU in the configuration cell; this has been dubbed Single Event Reconfiguration (SER). At the time of this printing, all of this new data has not yet been analyzed. Some of the results are discussed below, others are included in the tables, and others will be included in

the next edition. Please contact me if any additional information is immediately needed.

ACTELS AND PROTONS: Tests have been conducted on several models of the 1280 family for susceptibility to protons. Devices that would not upset under normal operating voltages (4.5 VDC < V_{CC} < 5.5 VDC) included the A1280, A1280A (both TI and Matsushita), and the 1280RP (A1280A repackaged by SEI). The RH1280's S-Module flip-flops did upset with protons and some data is shown in the figure below (from "Improved SEE Susceptibility of Radiation-Hardened ONO-Antifuse FPGA" presented at the 1996 SEE Symposium by J.J. Chang/Actel). Preliminary data on the S-Module flip-flops of the Act 3 A1460A indicates that it will not upset with protons. For comparison, the A1280XL 0.8 µm which is the same database as the RH1280, will be tested for proton upset in July.



RH1280 Proton Test Results

RH1280 AND SEDR: The antifuses on the RH1280 have been modified from the original commercial/military devices to harden them to Single Event Dielectric Rupture (SEDR). Essentially, the devices were thickened to decrease the electric field strength. The different thickness antifuses are ~85 Å for the commercial military devices and about 100 Å for the RH1280 (oxide-equivalent dimensions). Product testing by the foundry did not detect any evidence of SEDR. An initial NASA evaluation did detect SEDR and determined thresholds at several points. The data set taken was intentionally small so as not to seriously damage the parts; further data will be taken to get an accurate cross-section, which appears to be small. For S/N 068, the SEDR threshold for LET=37 was between 5.7 and 5.8 VDC, giving between 200 and 300 mV of margin for this part at room temperature. For S/N 063, the SEDR threshold for LET=53 was approximately 4.7 VDC, also at room temperature.

C-MODULE FLIP-FLOPS: In the last edition, the SEU performance of the various types of flip-flops was discussed. To expand on this, it should be noted that flip-flops implemented using 'C-Modules macros' may in fact be implemented in the combinational part of an S-Module. It is guaranteed by the design software that the dedicated flip-flop in the S-Module will not be used. This is critical since flip-flops made from C-Modules have superior SEU performance to those made from the dedicated flip-flops in the S-Modules. Testing appears to confirm this. Recently, a new chip design (CMOD2) has been tested at BNL to verify this and to quantify the SEU performance of the various configurations with data analysis expected to be completed in several weeks. For instance, an edge-triggered 'C-Module' flip-flop in a x1280y may be implemented by two C-Modules, two S-Modules, or a combination of S- and C-Modules. Also, single 'C-Module latches' may be implemented in a C-Module or the combinational part of a S-Module.

SUMMARY OF SEE PERFORMANCE OF VARIOUS FPGAs

Device	Feature Size	SEU Let th	Sat x-section	Temp
A1010	2.0	25	$5x10^{-6}$	R-->100C
A1020	2.0	25	$5x10^{-6}$	R-->100C
A1020A	1.2	25	$3x10^{-6}$	R
A1280 C	1.2	23	$3x10^{-6}$	R-->100C
A1280 S	1.2	5	$8x10^{-6}$	R-->100C
A1020B	1.0	28	$2x10^{-6}$	R
A1280A C	1.0	28	$2x10^{-6}$	R
A1280A S	1.0	5	$8x10^{-6}$	R
A1280A I/O In	1.0			
A1280A I/O Out	1.0	28		
A1280A 3.6V	1.0			R
RH1280 C	0.8	22	$8x10^{-6}$	R-->125C
RH1280 S	0.8	3	$9x10^{-6}$	R-->125C
RH1280 I/O In	0.8			
RH1280 I/O Out	0.8			
A1460A C	0.8		$\sim 2x10^{-7}$	R
A1460A S	0.8	>6	$1x10^{-6}$	R
A1460A I/O	0.8			
A1460A C 3.3V	0.8	~25	$8x10^{-7}$	R
A1460A S 3.3V	0.8	<6	$2x10^{-6}$	R
A1460A I/O 3.3	0.8			
Atmel AT6002	0.8	7-8		
Xilinx XC3090		4-7		
ATT2C04 config		< 7.88		
ATT2C04 data		> 10		

Device	Feature Size	SEL	SEDR	Clock Upset
A1010	2.0	NO		
A1020	2.0	NO	YES	Observed
A1020A	1.2	NO	YES	
A1020B	1.0	55	YES	
A1280	1.2	NO	YES	
A1280A	1.0	YES†	YES	
A1280A 3.6VDC	1.0	NO	NO	
A1280XL	0.8	NO	YES	
RH1280	0.8	NO	YES	
A1460A	0.8	NO	YES	
Atmel AT6002	0.8	~11		
Xilinx XC3090		4-7		
AT&T ATT2C04		< 7.88		
Quick Logic	0.6	< 60		

Notes: 1. A1460A Results same for routed global clocks and HCLK.

2. Cross-sections are in cm^2/flip-flop.

3. † Latchup detected only with MODE pin high (not flown in this configuration).

3. Single cell, C-Module latches have been tested but the data has not yet been analyzed.

4. Blank cells denote either 'not measured' or 'not yet observed.'

The obvious conclusions are:

1. Flip-flops made from two C-modules are relatively hard.

2. Flip-flops made from a single S-Module are relatively soft.

3. TMR techniques are required to make flip-flops very hard ($< 10^{-10}$ errors/bit-day)

4. A1020B devices are the only Actel devices known to latch up.

5. All the dielectric antifuse devices tested have shown susceptibility to SEDR. The RH1280 appears more resistant with its redesigned antifuse. Running at 3.6 VDC lowers the bias across the antifuse and no SEDR was observed for A1280A devices under these conditions.

6. RH1280 devices offer no significant improvement in SEU performance for C- and S-Modules.

7. 3.3 volt operation eliminates SEDR from Actels and increases SEU rate.

PROGRAMMING, DEBUGGING, and TESTING TIPS

HOT SOCKET: When using the debugger for either troubleshooting or running test vectors care should be taken not to remove parts when in the debugger menu system. In this state, a part will be removed from a powered socket and is not recommended.

BUG: It has been seen for certain lots of parts that the Activators will fail functional vectors on correctly working devices. This has been noticed in some A1280A lots. Troubleshooting has revealed that the Activator has trouble starting the parts with the voltage only reaching approximately 3.25 VDC. Additionally, current probing has found large (several hundred milliamp) current pulses going into the part in this mode. Lastly, when running the CHECKSUM command from the main menu, trouble starting the part was also observed with the DCLK input signal being clamped as a result of the reduced supply on the FPGA. Actel is currently working this problem.

HANDLE WITH CARE: The QFP172 package, used for the 1280 series, should be handled with care. A number of devices have come in with bent corners and these have had alignment problems with the Enplas ZIF sockets used on the Activators and test fixtures. The 'vacuum wand' should be used for removing parts from these sockets.

VERIFY ALL OF THE SPECIAL PURPOSE PINS. A number of cases have been seen where, for instance, the MODE pin has been left floating. This is very bad. As discussed, test procedures should ensure via direct measurement that the MODE pin is grounded. Additionally, pins such as V_{PP}, V_{SV}, V_{KS}, etc. should be checked as well as all power and ground pins. A completed instrument is currently being disassembled to fix floating MODE and V_{PP} pins.

DYNAMIC BURN-IN: Post-programming dynamic burn-in is a topic extensively discussed. Actel devices and SEI RAD-PAK devices both undergo dynamic burn-in with varying (widely) degrees of coverage. Along with the degree of coverage on the devices, there is also the fact that the parts are subject to relatively high voltages during programming. Responding to this, NASA has developed post-programming dynamic burn-in boards for the 1020 and 1280 families of parts. For each model, both quad-flat pack and pin grid array ZIF sockets are provided.

PACKAGE CONVERTERS: NASA has developed package converters for the QFP84 and the QFP172 flat packs to make them appear to be PGA84's and PGA176's. The converters are designed to be compatible with the '-repackage' command thus requiring no new placement and routing steps, preserving the database developed using PGA breadboard parts. Also, they give the capability to utilize existing ATE fixtures, radiation bias boards, etc., with quad flat pack devices. Lastly, they are useful for 'at-speed' testing of flight devices prior to lead forming and installation on the flight card.

ESD and LIDS: For a number of the Actel products, the lids are not grounded. It is imperative that proper precautions be taken to ensure that the parts are not damaged by ESD. There has been a number of cases where parts have been damaged in test. Failures have been reported in a burn-in oven others were on a parts tester at electrical test.

TOTAL DOSE PERFORMANCE AT LOW DOSE RATES

Testing of Actel A1280As has been completed under a number of dose rates. While there has been some variability, there has been no dramatic effect in performance vs. dose rate. Rockwell has tested a particular lot of A1280's (1.2 µm) at a rate of approximately 0.005 rads (Si) per second with results that indicated either different effects or an unusually 'hard' response for this type of device. In particular, they recorded data that showed only a minimal increase in I_{CC}: after 30 krads (Si) a delta of 2.1 mA and after 60 krads (Si) a delta of 3.2 mA.

Samples were tested at NASA/GSFC and at NASA/CalTech-JPL for a variety of dose rates with generally repeatable results for the A1280A product. However, none of the previous work tested at the 0.005 rads (Si)/sec rate. The first in our series of very low dose rate testing exposed an A1280A, PG176B, D/C 9424, U1H-82#21, PC423026 at a rate of 0.01 rads (Si) per second with a static bias. The total dose response of the device was similar to that obtained with higher dose rates. After approximately 10 krads (Si) of exposure, a delta current of approximately 70 mA was measured and at approximately 7 krads (Si) a delta current of 20 mA was measured.

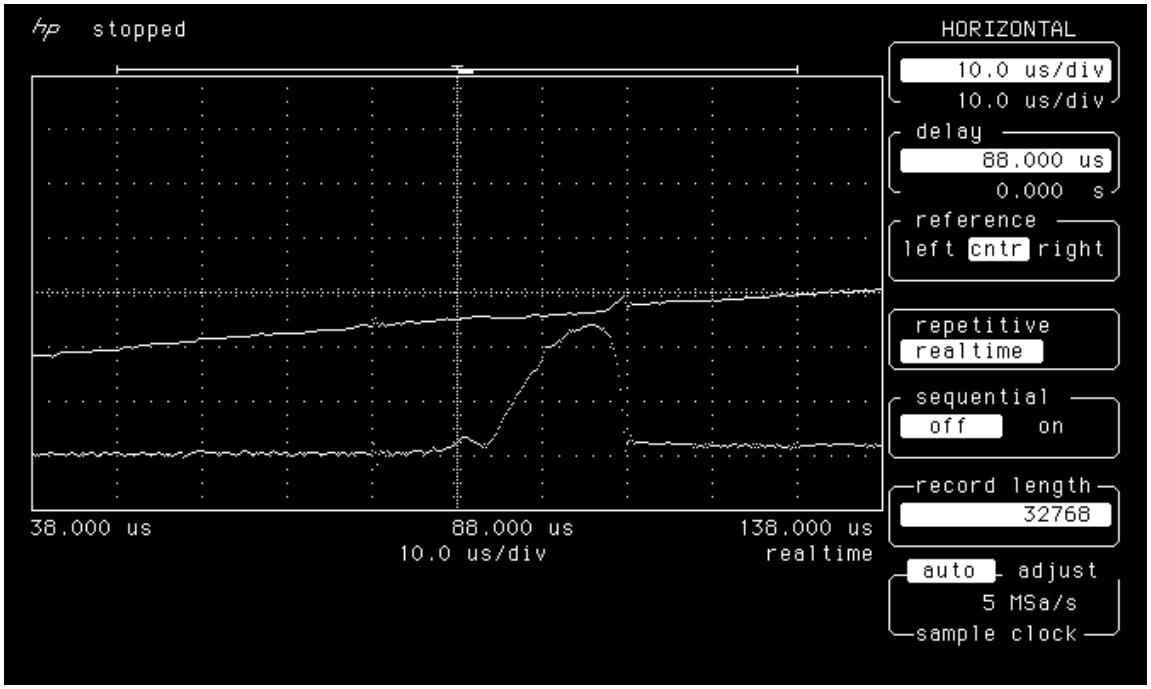
Currently, another sample is being tested at 0.002 ± 10% Rads (Si) per second, also under static bias. To date the device has been exposed to 7.2 krads (Si) with no change in supply current. Another device from the same lot of parts will be irradiated at 0.005 Rads (Si) per second using a dynamic bias board.

SUMMARY OF TOTAL DOSE PERFORMANCE

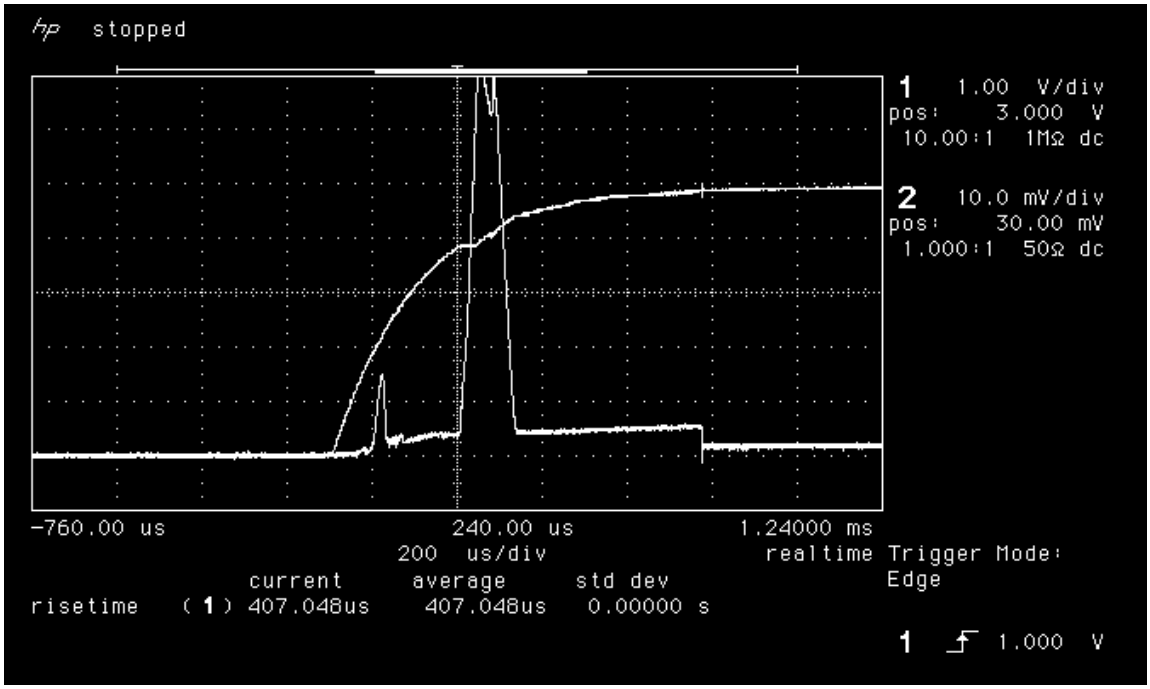
The charts below compiled by Gary M. Swift of CalTech/JPL show a summary of test results for many specific lots of A1280A's. A similar summary of A1020x's will appear in the next edition. Note that many components in the table do not include the results of annealing; thus, certain parameters such as I_{CC} and transient start-up currents will be less after annealing than is seen in the table. Post-annealing measurements are being made now.

Below is an example of the startup current characteristics of an A1280A. The first picture is from the control sample; the second is a device after 7 krads (Si) of radiation, post annealing. The two curves in the photo represent VCC at 1 V/DIV and ICC at 200 mA/DIV.

A1280A CONTROL SAMPLE



A1280A, 7 kRads (Si), Post-annealing



Voltage @ 1V/DIV, Current @ 100 mA/DIV

Summary of TID Test Results for the Actel A1280A

Tester	Date	Type	Method	Rate, rad(Si)/sec
Unisys	Apr-96	A1280A	only VLSI tester	0.02

	Wafer				Results, Icc for given krad(Si):			Remarks				
Date	s/n	Lot	#	DC	0	3	4	5	6	7	Anneal	(648 hrs at room temperature)
Apr-96	6-8	U1H403		9607	2.4mA	3.5mA	5.9mA	11mA	21mA	32mA	19mA	Note: worst of three parts
Apr-96	2-5	U1H335		9541	2.1mA	5.3mA	11mA	20mA	32mA	51mA	28mA	Note: worst of four parts

Tester	Date	Type	Method
NASA-G	May-96	A1280A	Post-irradiation-and-anneal current probe

					Startup Requirements			(after 7 krad(Si) and 648 hour room temperature anneal)
Date	s/n	Lot	#	DC	Icc, mA	Vcc, V	Time, us	Remarks
5/20/96	6-8	U1H403		9607	700 [240]	3.8 [2.6]	150 [16]	Note: worst of three parts, values in brackets are for unirradiated control (s/n:8)
5/20/96	2-5	U1H335		9541	870 [200]	180 [11]	3.9 [2.6]	Note: worst of four parts, values in brackets are for unirradiated control (s/n:1)

Tester	Date	Type	Method	Rate, rad(Si)/sec
NASA-J	Sep-95	A1280A	In-situ Icc + VLSI parameters	10

	Wafer				Results, krad(Si) for given Icc:			Startup Requirements after dose (in V, mA):			Remarks
Date	s/n	Lot	#	DC	Icc~40mA	Icc>80mA	Icc>100mA	4 krad	6 krad	8 krad	
9/10/95	110	U1H-80	38	9424	0	6.5	7.9	2.1, 70	3.4, 350	4.3, 580	
9/10/95	265	U1H-82*	21	9424	0	6.6	7.9	2.4, 150	3.3, 350	4.4, 680	* indicates no burn in
9/11/95	154	U1H-80*	38	9424	0	6.4	8	2.1, 70	--	4.8, 780	* indicates no burn in
9/11/95	202	U1H-82	21	9424	0	6.5	7.4	2.1, 90	--	4.7, 760	
9/13/95	102	U1H-80	38	9424	--	--	--	--	--	--	Not irradiated since fails pre-rad functionals
9/13/95	212	U1H-82	21	9424	0	6.6	8.4	2.1, 105	3.55, 320	4.6, 720	
9/14/95	103	U1H-80	38	9424	0	72mA @ 6	--	2.1, 70	3.5, 360	--	Irradiation stopped at 6 krad(Si)

Tester	Date	Type	Method	Rate, rad(Si)/sec
NASA-G	Jun-95	A1280A	In-situ Icc only with post-test VLSI	0.3

	Wafer				Results, krad(Si) for:			Remarks
Date	s/n	Lot	#	DC	Icc=40mA	Icc>80mA	Icc>100mA	
6/5/95	158	U1H-80*	38	9424	0	>>70	--	unbiased during irradiation to 70 krad(Si)
6/?/95	158	U1H-80*	38	9424	0	3.9	5.3	same part (previously irradiated unbiased), now biased
	three others (same lot) also tested							

Tester	Date	Type	Method	Rate, rad(Si)/sec
SEI	Mar-95	A1280A	only VLSI tester	6.3

	Wafer				Results, Icc for given krad(Si)					Remarks
Date	s/n	Lot	#	DC	3	5	6	7	8	
3/31/95	1-4	U1H250			x1	x2	x3	x4-5	x7-8	Note: values indicate times inital Icc

Tester	Date	Type	Method	Rate, rad(Si)/sec
Unisys	Mar-95	A1280A	only VLSI tester	0.03

	Wafer			Results, Icc for given krad(Si):					Remarks
Date	s/n	Lot	#	DC	0	5	10	Anneal	anneal was 96 hrs at room temperature
Mar-95	105-7	U1H-80	38	9424	2mA	12mA	80mA	50mA	Note: three parts tested
Mar-95	165	U1H-80*	38	9424	2mA	12mA	>250mA**	60mA	* indicates no burn in ** indicates part not starting
Mar-95	177	U1H-80*	38	9424	2mA	12mA	100mA	75mA	* indicates no burn in
Mar-95	178	U1H-80*	38	9424	2mA	12mA	80mA	60mA	* indicates no burn in

Tester	Date	Type	Method	Rate, rad(Si)/sec
Unisys	Jan-95	A1280A	only VLSI tester	.06-.02

	Wafer			Results, Icc for given krad(Si)							Remarks
Date	s/n	Lot	#	DC	0	5	10	15	20	Anneal	anneal was 384 hrs at room temperature
Jan-95	306-7	U1H83	9	9424	2mA	4mA	>64mA	85mA	>250mA**	105-120mA	Note: two parts
Jan-95	308	U1H83	9	9424	2mA	4mA	>64mA**?	>250mA**	>250mA**	>250mA**	** indicates part not starting
Jan-95	355-6	U1H83*	9	9424	2mA	4mA	>64mA	85-90mA	>250mA**	180-185mA	* indicates no burn in Note: three parts

Tester	Date	Type	Method	Rate, rad(Si)/sec
Unisys	Mar-94	A1280A	only VLSI tester	.03-.01

	Wafer			Results, Icc for given krad(Si)					Remarks
Date	s/n	Lot	#	DC	0	5	10	Anneal	anneal was 528 hrs at room temperature
Mar-94	3			9328	2mA	10mA	95mA	50mA	
Mar-94	5			9337	2mA	12mA	>500mA**	90mA	* indicates no burn in ** indicates part not starting
Mar-94	4,6-8			9337	2mA	12mA	100-120mA	50-95mA	Note: four parts tested

Tester	Date	Type	Method	Rate, rad(Si)/sec
NASA-G	Feb-94	A1280A	In-situ Icc only	0.3

	Wafer			Results, krad(Si) for:					
Date	s/n	Lot	#	DC	Icc=40mA	Icc>80mA	Icc>250mA	First "burp"	Remarks
Feb-94	008	U1H15		9337	0	8	12	15	"burp" means sudden, large current increase (to > 1 A)
	several others (same lot) also tested								

NASA run tests were run at either CalTech-JPL (NASA-J) or the Goddard Space Flight Center (NASA-G)

MISCELLANEOUS

Future work includes completing the characterization of the RH1280 and the A1460A. Additionally, testing is planned for the A14100A and the A32200DX devices.

A collection of papers and reports about Actel FPGAs will soon be released as a NASA report titled "Evaluation of Commercial Technology in Spacecraft Radiation-Hardened/High-Reliability Applications: A Case Study Using Field Programmable Gate Arrays." Contact either myself at GSFC or Gary Swift of CalTech/JPL (818) 354-5059 for availability.

ACKNOWLEDGEMENTS and REFERENCES

NASA/GSFC - Ken LaBel
(http://flick.gsfc.nasa.gov/radhome.htm)
NASA/JPL - Gary Swift

JET PROPULSION LABORATORY
PARTS ANALYSES

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Failure analysis and destructive physical analysis (DPA) has been performed on the following parts types. For a copy of the report, contact Joan Westgate (818-354-9529 or joan.c.westgate@jpl.nasa.gov) and request the desired log number.

Failure Analyses

Log#	MFR	LDC	PART DESC	PART NO.
6438	UTMC	9508A	Gate Array	12127-UT25ERISB
6553	ATC	8744	Capacitor, Ceramic, Chip	ATC 700
6614	OTK	9246	Optically Coupled Isolator	4N49
6620	Cannon	9240	Connector	ST11948-10N35PA
6621	Kemet	9347	Capacitor, Chip	CDR33BX104AKUS
6635	UTMC	9508A	Gate Array	12127-UT25ERISB
6647	UNI	9351	Driver, Power	UC1707

Destructive Physical Analyses

Log#	MFR	LDC	PART DESC	PART NO.	RESULT
6185	HON	9338	Gate Array	HR1060	Pass
6439	HON	9439	Gate Array	HR1060	Pass
6440	HON	9439	Gate Array	HR1060	Pass
6457	HON	9439	Gate Array	HR1060	Pass
6457	HON	9506	Gate Array	HR1060	Pass
6520	HPA	9527	Optocoupler	6N140	Pass
6545	NSC	9431	Line Driver	54AC241	Pass
6550	HPA	9518	Optocoupler	4N49	Pass
6556	HPA	9204	Optocoupler	6N140	Pass
6557	NSC	9420	Line Driver	54ACQ244	Pass
6558	NSC	9503	Line Driver	54AC240	Pass
6605	ADI	9517	Voltage Ref	AD2710	Fail
6617	FIL	0525	Filter	FN-1726	Fail
6617	FIL	0525	Filter	FN-1727	Fail

Manufacturers:

ADI	Analog Devices, Inc.	NSC	National Semiconductor Corp.
FIL	Filtronetics, Inc	OTK	Optek Technology, Inc.
HON	Honeywell	UNI	Unitrode
HPA	Hewlett Packard	UTMC	United Technologies Microelectronics Center

GODDARD SPACE FLIGHT CENTER PARTS ANALYSES

Listed below are the EEE parts analyses completed by the GSFC Parts Analysis Laboratory from 2/20/96 through 6/14/96. The Goddard Space Flight Center reports are available to NASA personnel and current NASA contractors by contacting your NASA project office.

Destructive Physical Analyses

Job Number	Manufacturer	Part Type	Part Number	Date Code	Result
62533	Hewlett Packard	Diode	JANTXV1N5711	9418	Pass
62532	Lakeshore Cryogenics	Diode, Temp Sense	S311-P-787	N/A	Fail
62530	Motorola	Diode	1N5314	9601	Pass
62529	Analog Devices	Microcircuit	5962-8777101MCA	9551	Pass
62528	AVX	Capacitor	87040-25	9613	Pass
62526	CDI	Diode	JANTXV1N4106-1	9524	Pass
62525	Microsemi Corp.	Diode	JANTXV1N6642	H9551	Fail
62520	Interpoint	Hybrid EMI Filter	5915-9500301HXA	9616	Pass
62519	APD	Diode	JANTXV1N4601-1	9146	Fail
62517	Microsemi Corp	Diode	JTXV1N6642U	H9449	Fail
62517	Microsemi Corp.	Diode	JANS1N6642U	9404B	Pass
62514	Q-Tech	Hybrid Oscillator	MCM2656-3M12.000MHz	9606	Fail
62513	National Semiconductor	Microcircuit	M38510/75203BCA	9603A	Pass
62511	Littlefuse	Fuse, FM08,125V 1A	FM08A125V1A	10982K	A
62508	McCoy	Hybrid Oscillator	M55310/19-B11A16M00000	9610J	Fail
62506	Harris Corporation	Transistor, FET	FRE9160R4R3949	9538	Pass
62504	Littlefuse	Fuse, FM08	FM08125V2A & 7A	96,119,612	Pass
62501	National Semiconductor	Microcircuit	M38510/75802SEA	9544	Pass
62500	Optek Technologies	Optocoupler	JANTXV4N24AU	9336	Fail
62499	Microsemi Corp (CCYL)	Diode, zener, 5.1V	JTXV1N6317	8946	Pass
62498	National Semiconductor	Microcircuit	5962-9218701M2A	9533A	Pass
62496	Harris Corp.	Transistor	FRL9130R3	9544	Fail
62495	Matra Harris	Microcircuit	MM4J67204EV-30/883	9608	Pass
62494	Optek Technologies	Optocoupler	JANTX4N22AU	9305	Pass
62490	UTMC	Microcircuit	R003E128W-JGSC	9405AA	Pass
62488	Harris Semiconductor	Microcircuit, Op-amp	5962-8962701PA	9531	Pass
62487	National Semiconductor	Microcircuit, Op-amp	5962-8962101PA	9542	Pass
62485	National Semiconductor	Microcircuit	5962-9218801M2A	9535A,9530D,9331A	Pass
62484	National Semiconductor	Microcircuit	5962-9217701M2A	9544A,9601A	Pass
62483	National Semiconductor	Microcircuit	M38510/11201BDA	9518G	Pass
62482	Q-Tech	Hybrid Oscillator	MCM2656-24.000MHZ	9421, 9520	Fail
62481	Leach	Relay	KCL-02A-002	8422, 8809	Fail
62480	National Semiconductor	Microcircuit	M38510/76302BEA	9606A	Pass
62479	AVX	Capacitor	87040-49	9516A	Pass
62475	Interpoint	Hybrid EMI Filter	FMH-461/SX	9540	Pass
62474	Actel	Microcircuit	5962-9215601MYA	9541	Fail
62473	Q-Tech	Hybrid Oscillator	MCM2656-3M12.000MHZ	9325, 9545	Fail
62472	Harris/IBM	Microcircuit	5962H9215301QXC	9332	Pass
62471	National Semiconductor	Microcircuit	M38510R75701BCA	9516A	Pass
62470	UTMC	Microcircuit	UG01GF84AISUA	9610	Pass
62468	Harris Semiconductor	Microcircuit	HS9-26C32RH-Q	9528	Pass
62467	Harris Semiconductor	Microcircuit	HS9-26C31RH-Q	9524A	Pass

62466	International Rectifier	Transistor	JANTXV2N7237	9411	Fail
62465	Actel	Microcircuit	A1280ACQ172C	9607	Fail
62464	Actel	Microcircuit	A1280ACQ172C	9607	Fail
62463	Interpoint	Hybrid DC-DC	5962-9306801HZA	9549	Fail
62460	SEI	Microcircuit	28C010TRPFB	9543	Pass
62459	National Semiconductor	Microcircuit	M38510/75602B2A	9335A	Pass
62458	National Semiconductor	Microcircuit	M38510/75503B2A	9312A, 9221A	Pass
62457	Teledyne	Hybrid	5150440-1	9526	Pass
62456	Teledyne	Hybrid	5150439-1	9529	Fail
62455	Teledyne	Hybrid	5150438-1	9526	Fail
62454	Teledyne	Hybrid	5150437-1	9526	Pass
62453	Teledyne	Hybrid	5150436-1	9526	Fail
62452	Teledyne	Hybrid	5150435-1	9526	Pass
62451	Texas Instruments	Microcircuit	5962-87739012A	9535L	Pass
62450	Harris Semiconductor	Microcircuit, SRAM	5962H9215301QXC	9335	Pass
62449	National Semiconductor	Microcircuit	5962-9219601M3A	9420A, 9542A	Pass
62448	National Semiconductor	Microcircuit	5962-9218401M2A	9431A	Pass
62447	National Semiconductor	Microcircuit	5962-9217601M2A	9547A	Pass
62445	Harris Semiconductor	Microcircuit	5962R9674201QEC	9550AAA	Pass
62444	National Semiconductor	Microcircuit	5962-9218301M2A	9602A	Pass
62443	Linfinity	Diode Array	JANTX1N6510	9350	Pass
62441	Optek Technology, Inc.	Transistor Array	JANTX2N6989U	9525	Pass
62439	Optek Technology, Inc.	Hall Effect Sensor	OMH3020B	9512	Pass
62438	Analog Devices (PMI)	Microcircuit	5962-8967001CA	9519	Pass
62437	AVX	Capacitor, Stack	87106-085	9547A, 9604A	Pass
62436	Kemet	Capacitor	M39014/01-1330	9017L	Pass
62435	National Semiconductor	Microcircuit	M38510/75703SRA	9450	Pass
62428	SEI (Actel)	Microcircuit	1280ARPQB	9551	Fail
62427	UTMC	Microcircuit	5962-8957701ZA	9552	Fail
62426	Ohmtek	Resistor Network	87016A1001FC	9420	Pass
62420	Solid State Electronics	Transistor	2N5552	9604	Fail
62419	Linfinity	Diode, Array	JANTXV1N5770	8906B	Pass
62418	Motorola	Microcircuit	M38510/30004B2A	9513	Fail

Failure Analyses

Job Number	Manufacturer	Part Type	Part Number	Date Code
62353	IBM		70163 LUNA-C	
62382	ACC		1331577	
62402			MHF28+12D	
62422		Microcircuit	Microcircuits	
62423	SEI	Microcircuit	7820RPDB	9234
62423	NSC	Microcircuit	JM38510-11202BPA	9417A
62424	Airborn	Connector	M83513/01-AN	9437
62425	PMI	Microcircuit	5962-8954101CA	A9435
62431		Connector	RMD63-00E/5-61P(801)	9542
62432		Connector	184-pin Connector	
62478	Spectra Diode Labs	Diode	SDL-5601-V1	
62489	Leach	Relay	KCL-2DA	unknown
62497	Littelfuse	Fuse	Fuse	
62505	Deutsch	Relay	TLS26M601	9451

Evaluations

Job Number	Manufacturer	Part Type	Part Number	Date Code
63521	Precision Circuits		3284480-1 Rev. C	1396
62440D	Cincinnati Electronics		520087-1	9534
62442	Potter & Brumfield	Relay	HL-4506	90/31
62486	NSC	Microcircuit	LF11202D	8831D
62486	Teledyne	Relay	422D Series	8939

GIDEP & NASA ADVISORY IMPACT REPORT

NASA Advisories, GIDEP Alerts, Problem Advisories, Safe Alerts, Product Change Notices, Diminishing Source Notices and Agency Action Notices related to EEE parts
March - June, 1996

Document #	Date	Part No.	Mfr.	Summary / Part Type
AAN-U-96-39	3/21/96	Multiple	N/A	The Naval Ordnance Center is disseminating a safety advisory about Army and Navy non-rechargeable, dry, primary, lithium batteries. The batteries have exploded during routine disposal discharges and routine state-of-charge checks using a state-of-charge meter due to overheating.
AH6-D-96-04	2/28/96	NM93CS66J-SMD, 5962-9154901MPA	National.	The manufacturer is discontinuing subject microcircuits.
AH6-C-96-06	3/6/96	MIL-PRF-38535	National	This process, product or package change notification is published per the requirements of MIL-STD-883 and is provided for your information and use.
BN8-A-96-02	3/8/96	82S191/BJA , 5962-01-360-8256	Philips Semiconductor	Customer reporting functional failure at -55C during power strobe testing on specific codes after a 2 hour preconditioning soak at -55C. This test is a custom requirement, not a data sheet parameter.
BP6-C-96-05A	2/28/96	N/A	Harris Corp.	The manufacturer is issuing this amendment to clarify it's position as regards GSI and CSI inspections on radiation hardened microcircuits
CE9-C-96-08	2/28/96	SNJ54ABT841	Texas Instruments	This notice is being published to notify customers of recent datasheets changes to the manufacturers military integrated circuits.
CE9-C-96-09	3/6/96	Multiple	Texas Instruments	Under the provisions of MIL-PRF-38535, the manufacturer has eliminated 100% temperature cycle and constant acceleration on the subject chip carriers.
CE9-P-96-02	3/13/96	Multiple	Texas Instruments	This advisory describes a specific application condition that should be avoided when using the 16megabit DRAMS packaged parts which use the 16ms rev p1.4 die.
EA-D-96-17	3/6/96	59501-80092 , 5950-01-309-3974	Hewlett-Packard	Defense Electronics Supply Center (DESC) is reporting the discontinuance of the listed part number and the associated national stock number.

Document #	Date	Part No.	Mfr.	Summary / Part Type
EE-A-96-01	**3/6/96**	**LH0021K , 5962-00-374-8196**	**National**	**The manufacturer has confirmed a wire bonding anomaly from the post and die to the substrate on hybrid integrated circuit of Lockheed Martin Control Systems (LMCS) drawing number 144A9562PL. The anomaly to date has been restricted to lot date code 9441 that was manufactured off-shore in Singapore. LMCS has been identified as the only customer in receipt of this date code. However, internal gas analysis results cast suspicion on date codes 9447 and 9450. The manufacturer believes that the cause of the anomaly is related to leaking glass lead seals. Upon further investigation, parts were determined to contain chlorine along with high levels of moisture (>10,000ppm). The elevated moisture level and chlorine contamination within the package directly contribute to dangerous corrosion.**
GG4-A-96-01	**2/28/96**	**JANTXV2N5154 , 5961-01-338-3611, MIL-S-19500/544**	**PPC Products Corp.**	**PPC Products Corp. received notification from Space Systems Loral of an anomaly encountered with PPC devices lot date code 9406. Loral selected three samples for DPA, two out of three of the collector leads came off during DPA handling. The correspondence states that "normally these leads are strong enough to withstand handling received during DPA". This problem has not been reported by any other customer, and PPC is confident that this is an isolated case. the product in question passed all incoming inspection and screening requirements including group C subgroup 2 terminal strength to method 2036. However the product was recalled in October of 1995 for an unrelated problem, reference GIDEP alerts SF-A-95-01 and SF-A-95-02A.**
SF-A--95-02A	**2/28/96**	**JANTXV2N5153 , 5961-01-337-8554 , MIL-S-19500/545**	**PPC Products Corp.**	**A DPA sample of five transistors from date code 9349 was subjected to RGA tests per MIL-STD-883, method 1018, procedure 1. Three of five transistors failed the RGA tests for high moisture content, exceeding the 5000 ppm limit of MIL-S-19500.**
VV-D-96-02	**3/6/96**	**Multiple**	**Thomson Components and Tubes Corp.**	**The manufacture is discontinuing subject microcircuits.**
VV-D-96-09	**3/8/96**	**Multiple**	**Burr-Brown Corp.**	**The manufacture is discontinuing subject microcircuits.**

Document #	Date	Part No.	Mfr.	Summary / Part Type
VV-D-96-10	3/8/96	87Z3 , 5985-00-124-9953	Andrew Corp.	The manufacture is discontinuing subject (splice) part numbers and national stock number. The referenced part number was obsoleted in June 1995.
VV-D-96-10A	3/11/96	87Z3 , 5985-00-124-9953	Andrew Corp.	This amendment contains additional information that identifies the DESC case number, the user response deadline date and the federal point of contact.
VV-D-96-11	3/14/96	Multiple	Integrated Device Technology	The manufacture is discontinuing subject microcircuits.
VV-D-96-12	3/19/96	Multiple	Advanced Micro Devices Inc.	The manufacture is discontinuing subject microcircuits.
AAN-U-96-39A	4/18/96	Multiple	N/A	This is a follow up advisory about Army and Navy non-rechargeable, dry, primary, lithium batteries. The additional information and guidance is related to the following areas: A. NSN's of affected batteries, replacement batteries and support hardware. B. An alternative method for preparing affected batteries for disposal . C. Guidance for proper disposal of affected batteries. D. Reporting requirements for malfunctioning batteries.
AH6-D-96-05	4/ 2/96	Multiple	National	Manufacturer is discontinuing subject microcircuits.
AH6-D-96-06	4/22/96	Multiple	National	Manufacturer is discontinuing subject microcircuits.
AK-P-96-01	4/ 5/96	MIL-W-16878/4	Cal-Pacific Electronics Corp.	During adjustment of a potentiometer, four radial cracks through the red/black teflon insulation were observed on the wire which connects to the potentiometer. These cracks, all within a six inch length, exposed the wire's conductor strands. The red/black wire is one of six different colored wires on the potentiometer. All other wires were found to be acceptable. All the wires are silver-plated, multiple-strand copper wires with teflon insulation, manufactured to MIL-W-16878/4.

Document #	Date	Part No.	Mfr.	Summary / Part Type
CE9-C-96-10	**4/ 4/96**	**Multiple**	**TI**	**The manufacturer is notifying it's customers of recent changes to it's military integrated circuits. These changes are all fully qualified to military requirements and approved by it's Technology Review Board (TRB). Qualification data is kept on file. Where it has been determined that customer source control drawings are affected, these customers will be contacted directly for any change approvals.**
CE9-C-96-11	**4/ 4/96**	**Multiple**	**TI**	**The manufacturer is notifying it's customers of recent changes to it's military integrated circuits. These changes are all fully qualified to military requirements and approved by it's TRB. Qualification data is kept on file. This change refers to the manufactures datasheet device. If the change affects a DESC SMD or JAN slash sheet, notification of the change will be issued by DESC. If the change affects a customer's SCD, The manufacturer will contact these customers directly for needed approvals.**
CE9-C-96-12	**4/23/96**	**Multiple**	**TI**	**Under the provisions of MIL-PRF-38535, the manufacturer has eliminated 100% burn-in on the subject microcircuits.**
CE9-C-96-13	**4/23/96**	**Multiple**	**TI**	**The manufacturer is notifying it's customers of recent changes to it's military integrated circuits. These changes are all fully qualified to military requirements and approved by it's TRB. Qualification data is kept on file. This change refers to the manufactures datasheet device. If the change affects a DESC SMD or JAN slash sheet, notification of the change will be issued by DESC. If the change affects a customer's SCD, The manufacturer will contact these customers directly for needed approvals.**
CE9-P-96-03	**4/ 2/96**	**5962-7802004MFA**	**TI**	**This advisory describes a symbol issue specific to the part and package type listed below. This SMD was converted to add the 5962 prefix to the symbol in December of 1993. At that time the traveler was updated to reflect the addition of 5962 to the symbol requirements. In subsequent traveler changes in October of 1995 the traveler was inadvertently tied to the old symbol diagram which did not have the 5962 prefix. This was found and corrected in February of 1996. Review of shipping history shows that three date codes of parts were built and shipped using the old symbol formats. date codes affected were 9542A, 9542B and 9551C.**

Document #	Date	Part No.	Mfr.	Summary / Part Type
E3-P-96-01	**4/18/96**	**Multiple**	**Amphenol Corp.**	**The subject devices are no longer on QPL. They have been canceled since January 1, 1992. The manufacturer is continuing to supply some items from the above listed series marked with item identification numbers identical to those used previously to identify the MIL QPL'd items. Be advised that no MIL screening is accomplished on these items.**
G2-P-96-01	**4/12/96**	**JANS2N3439/AAT05D3439, MIL-S-19500/368**	**PPC Products Corp.**	**Honeywell Space and Strategic Operations experienced 3 failures OF the manufacturers low power transistor during subassembly testing. Board level fault isolation determined the cause of the anomalies was excessive transistor leakage. All 3 parts were removed and the Honeywell failure analysis lab verified 2 of the 3 parts (PPC D/C 9426, L/N 94-178) had open internal wires due to melt through . The third part was successfully tested at room temperature without incident.**
VV-D-93-13	**4/ 1/96**	**AM8530H-4, AM8530H-6 , AM8530H-8, 5962-01-346-1522**	**Advanced Micro Devices**	**Manufacturer is discontinuing subject microcircuits.**
VV-D-93-14	**4/ 1/96**	**Multiple**	**Altera Corp.**	**Manufacturer is discontinuing subject microcircuits.**
VV-D-96-15	**4/ 1/96**	**Multiple**	**Altera Corp.**	**Manufacturer is discontinuing subject microcircuits.**
VV-D-96-16	**4/22/96**	**Multiple**	**Allegro Micro Systems**	**Manufacturer is discontinuing subject microcircuits.**
VV-D-96-17	**4/24/96**	**Multiple**	**Siliconix**	**Manufacturer is discontinuing subject microcircuits / transistors.**
AH6-C-96-07	**5/13/96**	**Multiple**	**NSC**	**This process flow, and test limit change notification is published per the requirements of MIL-STD-883.**
AH6-D-96-07	**5/15/96**	**Multiple**	**NSC**	**Manufacturer is discontinuing subject semiconductors.**
VV-D-96-21	**5/13/96**	**Multiple**	**DARE Electronics Inc.**	**Manufacturer is discontinuing subject microcircuits..**
VV-D-96-21A	**5/15/96**	**Multiple**	**DARE Electronics Inc.**	**The manufacture is discontinuing the following components - coil assembly, board and contact, visor, cathode ray, electrical chassis, electrical solenoid.**

Document #	Date	Part No.	Mfr.	Summary / Part Type
B8-A-96-01	**5/16/96**	**RWR82S1R43FR**	**TEPRO of Florida, Inc.**	**Four d/c 9550 MIL-R-39007 wire wound, 1.43 ohm, 1%, 1.5w resistors exhibited high resistance after board assembly and ESS temperature cycling. Circuit operation at ambient temperature and at ESS temperature extremes included the activation of resistive loads by applying current pulses through these resistors. Two failures were depotted and exhibited resistor wire to end cap weld separation. Optical and SEM indicate clean separation with no metal attach residuals at the weld site. Five 1.43 ohm d/c 9550 resistors were pulled direct from inventory, and one additional high resistance failure was discovered. As part of this investigation, TSD requested that the manufacture submit ten uncoated resistors for weld analysis. A quantity of twelve was received and under medium power (10x to 40x) magnification, most exhibited questionable weld quality; such as compressed / deformed end caps at the weld site, weld slag/splatter, wire / weld flattened to a suspiciously thin cross section, wire dress / routing after the weld following a path almost touching the edge of the end cap, highly variable weld patterns / shapes.**
BP6-C-96-10	**5/3/96**	**Multiple**	**Harris**	**The manufacturer is issuing this product change notice to advise you of a wafer fabrication change on digital products.**
CM2-D-96-01	**5/14/96**	**Multiple**	**Analog Devices Inc.**	**Manufacturer is discontinuing subject microcircuits..**
DT6-D-96-02	**5/1/96**	**Multiple**	**Motorola**	**Manufacturer is discontinuing subject microcircuits..**
VV-D-96-11A	**5/8/96**	**Multiple**	**Integrated Device Technology Inc.**	**Manufacturer is discontinuing subject microcircuits (additional information received).**
VV-D-95-17A	**5/9/96**	**Multiple**	**Advanced Micro Devices**	**Manufacturer is discontinuing subject microcircuits (additional information received).**
VV-D-96-18	**5/1/96**	**Multiple**	**Altera Corp.**	**Manufacturer is discontinuing subject microcircuits..**
VV-D-96-20	**5/13/96**	**Multiple**	**BKC Semiconductor**	**Manufacturer is discontinuing subject microcircuits..**

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